2011-09

Preconditioner circuit analysis

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NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

PRECONDITIONER CIRCUIT ANALYSIS

by

Matthew J. Nye

September 2011

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REPORT DOCUMENTATION PAGE			Form Approved OMB No. 07040–188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 222024–302, and to the Office of Management and Budget, Paperwork Reduction Project (07040–188) Washington DC 20503.			
1. AGENCY USE ONLY *(Leave blank)*	**2. REPORT DATE** September 2011	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE Preconditioner Circuit Analysis			**5. FUNDING NUMBERS**
6. AUTHOR(S) Matthew J. Nye			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 939435–000			**8. PERFORMING ORGANIZATION REPORT NUMBER**
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A			**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. IRB protocol number: N/A.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited			**12b. DISTRIBUTION CODE**

13. ABSTRACT (maximum 200 words)

Voltages up to 10,000 volts or higher must be attenuated and measured to provide control feedback for many applications like medium voltage generators or pulsed power systems. How these medium voltage signals can be conditioned so that they can be input to analog control circuits or analog-to-digital converters is the focus of this thesis. A preconditioner circuit takes as input a medium voltage signal and outputs a low voltage conditioned signal to an analog-to-digital converter. Each of the components of the preconditioner circuit, a voltage divider and an averaging circuit designed with an operational amplifier, contributes to the signal conditioning. The theoretical computations, simulations of the circuit, and experimental data were analyzed for congruence. The 3 dB bandwidth of the experiment's frequency response was significantly reduced compared to that of the simulation's frequency response because of parasitic capacitances in the circuit board.

14. SUBJECT TERMS Preconditioner Circuit, Analog-to-Digital Converter, Voltage Divider, Averaging Circuit, AD8027 Amplifier			**15. NUMBER OF PAGES** 87
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UU

NSN 75400–12–805–500

Standard Form 298 (Rev. 28–9)
Prescribed by ANSI Std. 2391–8

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Approved for public release; distribution will be unlimited

PRECONDITIONER CIRCUIT ANALYSIS

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
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ABSTRACT

Voltages up to 10,000 volts or higher must be attenuated and measured to provide control feedback for many applications like medium voltage generators or pulsed power systems. How these medium voltage signals can be conditioned so that they can be input to analog control circuits or analog-to-digital converters is the focus of this thesis. A preconditioner circuit takes as input a medium voltage signal and outputs a low voltage conditioned signal to an analog-to-digital converter. Each of the components of the preconditioner circuit, a voltage divider and an averaging circuit designed with an operational amplifier, contributes to the signal conditioning. The theoretical computations, simulations of the circuit, and experimental data were analyzed for congruence. The 3 dB bandwidth of the experiment's frequency response was significantly reduced compared to that of the simulation's frequency response because of parasitic capacitances in the circuit board.

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TABLE OF CONTENTS

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LIST OF FIGURES

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LIST OF TABLES

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EXECUTIVE SUMMARY

In this thesis, a signal preconditioner circuit which converts a medium voltage input into a low voltage signal to drive an analog-to-digital converter was analyzed. A signal preconditioner circuit has many applications in electronics. Voltages up to 10,000 volts or higher must be attenuated and measured to provide control feedback for many applications like medium voltage generators or pulsed power systems. How these medium voltage signals can be conditioned so that they can be input to analog control circuits or analog-to-digital converters is the focus of this thesis.

Two experiments are carried out to analyze the response of the signal preconditioner circuit. In the first experiment, a high voltage signal is connected to the voltage divider of the circuit through an isolation transformer to analyze the attenuation of the signal and the output signal from the amplifier. In the second experiment, a low voltage signal is connected directly to the averaging circuit to analyze the frequency response of the amplifier.

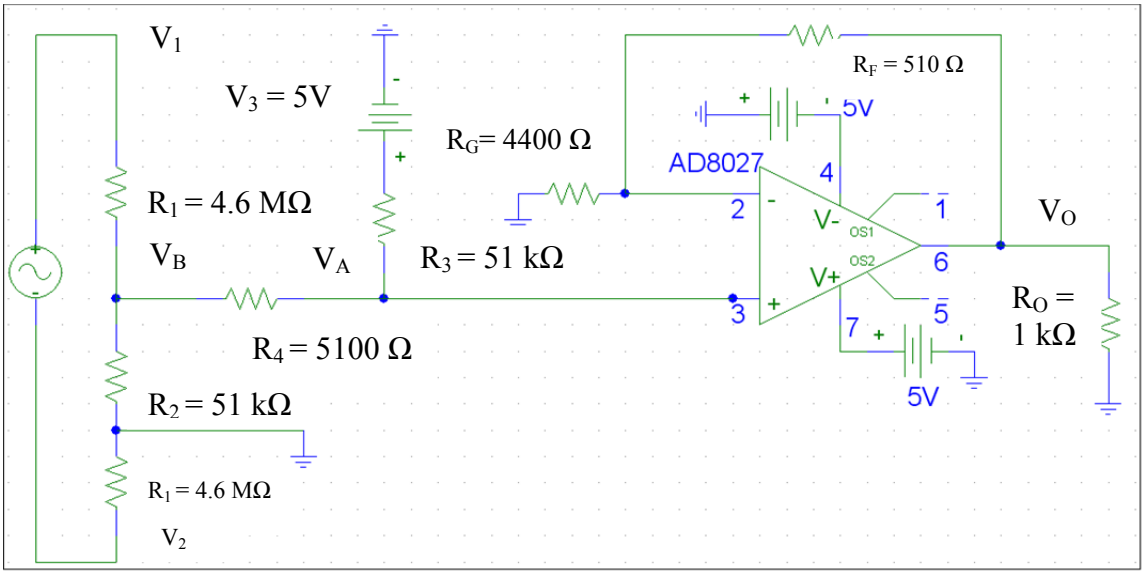
A preconditioner circuit takes as input a medium voltage signal and outputs a low voltage conditioned signal to an analog-to-digital converter. The signal preconditioner circuit, shown on the next page, has three sections. The first section consists of three resistors that form a voltage divider. The voltage divider of the signal preconditioner circuit attenuates the medium voltage input to a low voltage input for the amplifier.

In the second section of the circuit, the voltage divider branch and a DC offset branch connect to the noninverting terminal of an AD8027 operational amplifier. These two branches together form a passive averaging circuit and make up the second section of the signal preconditioning circuit. These two branches are combined to produce an average output signal of both branches.

In experiment one, the voltage for the voltage divider branch input is 120 volts root mean square (rms). This source is galvanically isolated from the low voltage circuit through an isolation transformer, as will be the case in any application. The supply

voltage for the second experiment is a one volt peak-to-peak sine wave with a 0.5 volt DC offset. The other branch in both experiments is a single resistor with a supply voltage of 5.0 volts DC.

The passive averaging circuit connects to an amplifier which is the third part of the signal preconditioner circuit. The high input impedance of the amplifier is essential to prevent loading on the voltage divider. Without the amplifier in the circuit, the lower input impedance of the analog-to-digital converter causes the input current to the analog-to-digital converter to change the measured voltage. The feedback loop is connected from the output of the amplifier through a resistance to the inverting terminal of the amplifier. The resistor R_G from the inverting terminal of the amplifier to ground is ideally infinite so that the operational amplifier gain is unity. The preconditioner circuit for Experiment 1 is shown below.



Preconditioner Circuit for Experiment 1.

In both experiments the mean output voltage and peak-to-peak output voltage from the oscilloscope were compared with theoretical computations and simulations of the circuits. The mean output voltage and peak-to-peak output voltage from the experimental data, simulations, and theoretical computations were approximately equal. However, the frequency response from Experiment 2 was significantly attenuated relative to that of the simulation of the circuit as a result of unaccounted for parasitic capacitances

in the experiment's circuit board. When the parasitic capacitances were added to the simulation's schematic, the cutoff frequency matched that for the experimental results. The transfer function of the preconditioner circuit was modified with the addition of the parasitic capacitances. This modified transfer function was plotted, and the results matched both the experimental and simulation frequency responses.

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I. INTRODUCTION

A. MISSION

In this thesis, the operation of a signal preconditioner circuit is analyzed with both simulations and experiment. This circuit will be part of an isolated high voltage sensor for electric ship systems. Sensing voltages in electric drives and pulsed power weapons systems is critical for reliable and autonomous operation. The results of the simulations and experiments are compared to the theoretical results. From the results, the output and frequency response of the circuit are verified for accuracy.

B. OBJECTIVE

The signal preconditioner circuit has been utilized in the design phase for the power supply of ship systems. Commercially available voltage sensing test equipment is very expensive. This high voltage sensor concept realizes a more compact, cost effective means to measure high voltage for electric ship sensing requirements. There is no known product on the market with the features of this sensor, i.e., high voltage sensing that generates an isolated, digital output signal in real time. High voltage sensor concepts have been described, such as in [1], which is an alternative to a resistive voltage divider.

The goal of this research was to determine the reasons for a diminished 3 dB value from the circuit board's frequency response to that of simulated frequency response of the preconditioner circuit. Two experiments were designed to analyze the response of the signal preconditioner circuit. These two experiments tested the operation of every component of the signal preconditioner circuit, which includes a voltage divider, a passive averaging circuit, and an operational amplifier. In the first experiment, a high voltage signal, a 120 volts root mean square (rms) sine wave at 60 Hz, was connected to the voltage divider of the circuit with an isolation tranformer to analyze the attenuation of the signal and the output signal from the amplifier. The isolation transformer attenuates the voltage to 115 volts rms, and the voltage divider further attenuates the voltage to 0.868 volts peak. An isolation transformer is essential when higher voltages are applied to the circuit to prevent damage. If isolation is not used, then the AC ground creates a loop with the operation amplifier circuit ground. In the final application of this circuit,

the operational amplifier ground is isolated, and the output is delivered via fiber optics. In the second experiment, a low voltage signal, 1.0 volt peak-to-peak sinusoid with a mean value of 0.5 volts, is connected directly to the averaging circuit to analyze the frequency response of the amplifier. The frequency range tested for is from 10 to 5 MHz.

C. APPROACH

The first task in this thesis is to perform the theoretical computations for the various stages of the signal preconditioner circuit. The circuits for both of the experiments are then simulated, and the results are compared to the theoretical computations. These same circuits were then built and tested, and these measured results were compared to the results of the simulations and the theoretical computations.

D. THESIS ORGANIZATION

This thesis is organized into four chapters. The theoretical computations for every component of the signal preconditioner circuit, which includes the voltage divider, passive averaging circuit, and amplifier, are included in Chapter II. The experimental results and simulations are analyzed and compared with the theoretical computations in Chapter III. The procedures of both experiments are covered in Chapter IV, and the conclusions and future work recommendations are in Chapter V.

II. CIRCUIT ANALYSIS

A. REARRANGEMENT OF VOLTAGE DIVIDER BRANCH

In order to derive the transfer function for the voltage divider, an equivalent circuit is derived in this section. It is shown that the voltage divider can be rearranged to yield an equivalent circuit. All of the voltage divider current in the circuit of Figure 1 is flowing through R_1 and R_2, and only a negligible amount is flowing into the branch which is connected to the noninverting terminal of the operational amplifier. The high input impedance at the noninverting terminal of the amplifier draws little current. From the datasheet, the input impedance for the AD8027 amplifier is 6 MΩ. The circuit can be rearranged so that the two resistors marked R_1 are connected in series above node V_B. The current flowing into the amplifier's noninverting node is unchanged by placing the two R_1 resistors in series above node V_B. Figure 1 is the circuit for Experiment 1, and Figure 2 is the rearranged circuit with both resistors marked R_1 in series above node V_B.

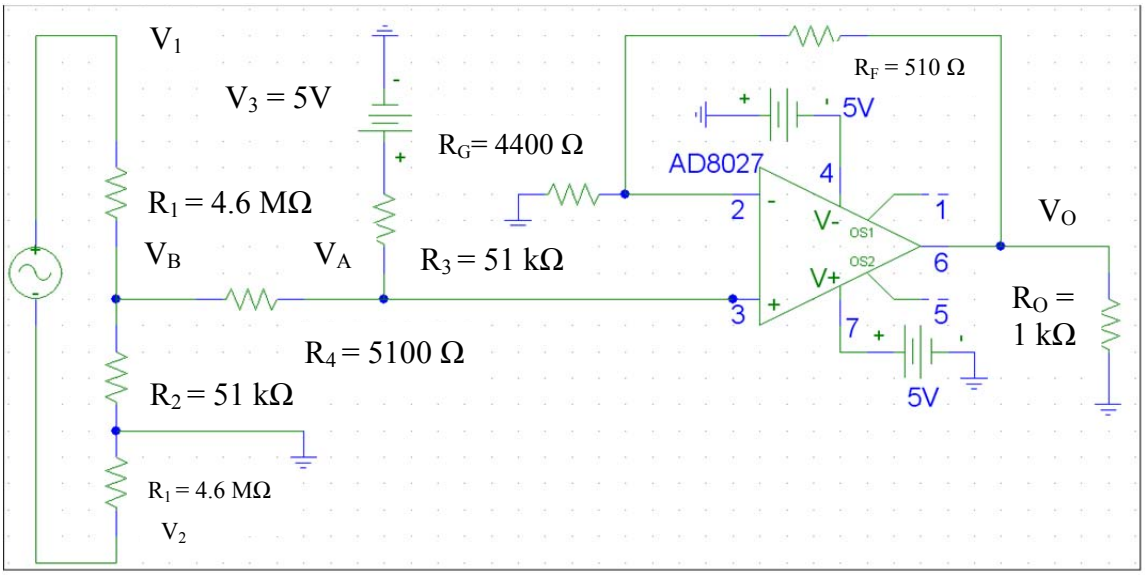

Figure 1. Preconditioner circuit for Experiment 1.

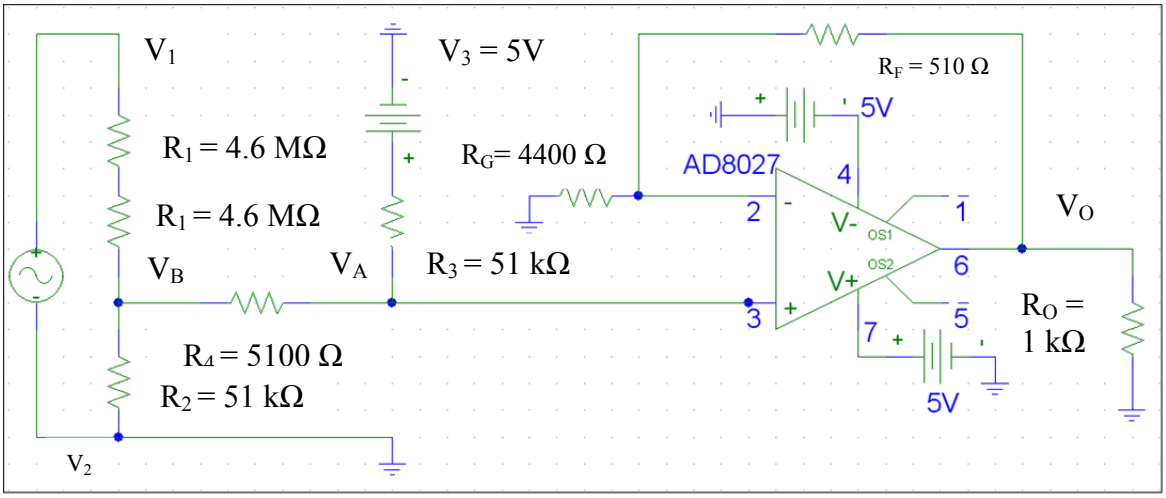

Figure 2. Rearranged preconditioner circuit for Experiment 1.

The two resistors marked R_1 in Figure 2 are in series above node V_B, sharing the same current, so the circuit depicted in Figure 2 is equivalent to the circuit shown in Figure 1. The circuit in Figure 1 was used in the first experiment, and the circuit in Figure 2 was only used for analysis purposes.

B. DETERMINATION OF THE THÉVENIN EQUIVALENT CIRCUIT OF THE VOLTAGE DIVIDER USING NODAL ANALYSIS

We will simplify the voltage divider section of the circuit shown in Figure 2 to its Thévenin equivalent circuit. We want to represent the voltage divider section as the equivalent single voltage source and single resistor. The Thévenin equivalent circuit is a simplification technique used in circuit analysis. We want to find the Thevenin equivalent for the voltage at V_B. The ground reference for the signal conditioning circuit is V_2. We want to focus on the behavior of these terminals as the input voltage V_1 is adjusted.

The first step is to determine the Thévenin voltage V_{Th} which is simply the open-circuit voltage in the original circuit at V_B. We make the load resistance infinitely large so that we have an open-circuit condition at V_B. The Thévenin voltage is calculated with a voltage divider at V_B which is calculated in

$$V_{Th} = V_{OC} = \frac{V_1 - V_2}{2R_1 + R_2} R_2. \tag{1}$$

From Figure 3, the load resistance to the right of V_B can be seen as infinite giving an open-circuit condition at V_B.

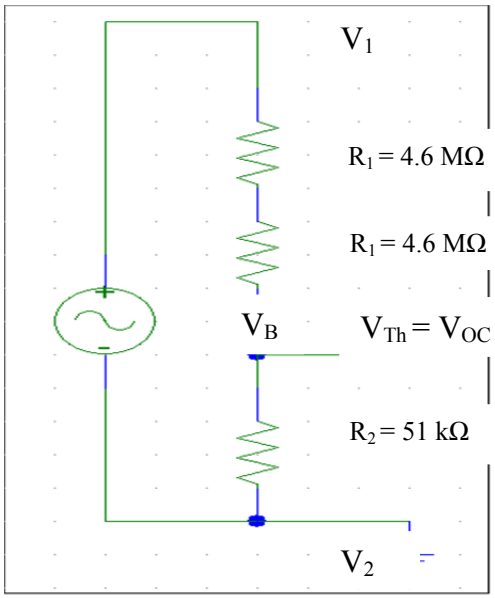

Figure 3. Circuit used to calculate Thévenin voltage.

We next determine the short-circuit current i_{SC} by placing a short from V_B to V_2 which is connected to ground. This causes the current to bypass R_2. The short circuited current still flows through the R_1 resistors. From Figure 4, a short between V_B and V_2 can be seen that causes all the current to bypass R_2. The short circuited current is calculated from

$$i_{SC} = \frac{V_1 - V_2}{2R_1}. \tag{2}$$

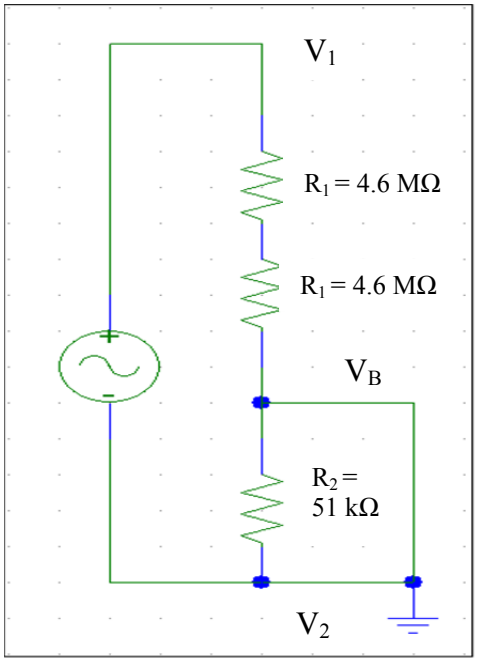

Figure 4. Circuit used to determine short-circuit current.

The Thévenin resistance is the ratio of the open-circuit voltage to the short-circuit current. The Thévenin resistance is calculated by substituting (1) and (2) into

$$R_{Th} = \frac{V_{Th}}{i_{sc}} = \frac{\frac{V_1 - V_2}{2R_1 + R_2} R_2}{\frac{V_1 - V_2}{2R_1}} = \frac{2R_1 R_2}{2R_1 + R_2}. \tag{3}$$

The R_1 and R_2 resistors in the circuit are reduced to an equivalent Thévenin voltage and Thévenin resistance [2]. This simplified Thévenin branch and the V_3 branch in Figure 2 make a passive averaging circuit and are shown in Figure 5. Figure 5 is a representation of a passive averaging circuit because it averages the voltages of the two branches feeding the noninverting terminal [3].

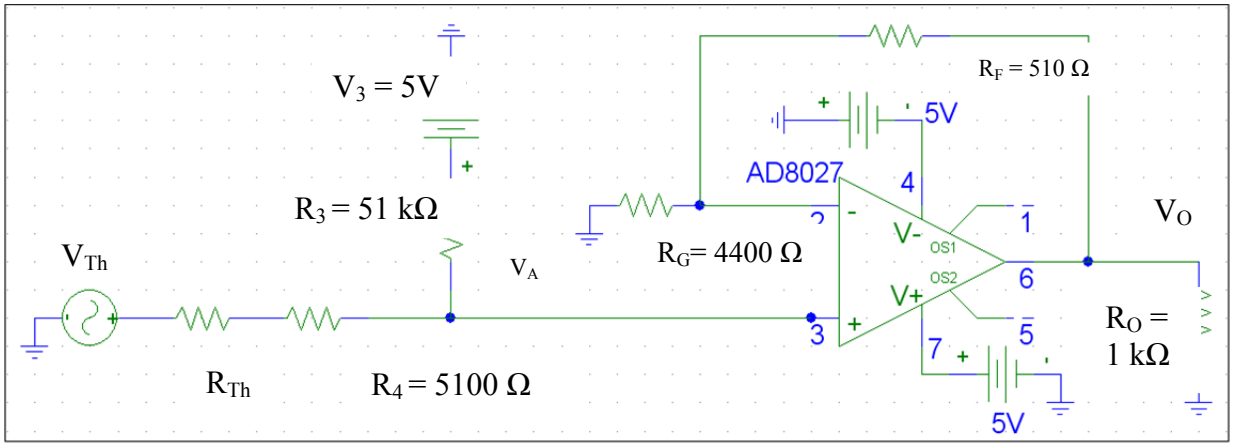

Figure 5. Thévenin equivalent circuit for preconditioner circuit.

The following equations show the steps in deriving an output voltage for the averaging circuit using the Thévenin equivalent circuit shown in Figure 5.

Nodal analysis at node V_A of the circuit shown in Figure 5 yields

$$\frac{V_{Th}-V_A}{R_{Th}+R_4}+\frac{V_3-V_A}{R_3}=0. \tag{4}$$

The terms including V_A are moved to the left hand side of (4) to get

$$V_A\left(\frac{1}{R_{Th}+R_4}+\frac{1}{R_3}\right)=\frac{V_{OC}}{R_{Th}+R_4}+\frac{V_3}{R_3}. \tag{5}$$

Solving for V_A on the left side of (5), we get (6), the output voltage of the averaging circuit:

$$V_A=\frac{\left(\frac{V_{OC}}{R_{Th}+R_4}+\frac{V_3}{R_3}\right)}{\left(\frac{1}{R_{Th}+R_4}+\frac{1}{R_3}\right)}. \tag{6}$$

Next, a nodal analysis is done at the inverting terminal of the operational amplifier. The voltage at the inverting terminal is V_A. The voltages at both terminals are

assumed to be equal because the operational amplifier is assumed to be an ideal operational amplifier [4]. This nodal analysis gives

$$\frac{V_O - V_A}{R_F} + \frac{0 - V_A}{R_G} = 0. \tag{7}$$

The term V_O in (7) is moved to the left hand side to get

$$\frac{V_O}{R_F} = V_A\left(\frac{1}{R_F} + \frac{1}{R_G}\right) = V_A\left(\frac{R_F + R_G}{R_F R_G}\right). \tag{8}$$

Multiplying both sides of (8) by R_F, we see that the R_F terms cancel on both sides, and

$$V_O = V_A\left(\frac{R_F + R_G}{R_G}\right). \tag{9}$$

Equation (6) is then substituted into (9), which eliminates V_A from the expression, to get

$$V_O = \left(\frac{R_F + R_G}{R_G}\right)\left[\frac{\left(\frac{V_{Th}}{R_{Th} + R_4} + \frac{V_3}{R_3}\right)}{\left(\frac{1}{R_{Th} + R_4} + \frac{1}{R_3}\right)}\right]. \tag{10}$$

Equation (10) gives the output voltage in terms of the two input voltages and the resistances of the circuit. The output voltage of (10) can be easily predicted because the equation has only constant voltages and resistances in it. However, there are frequency varying impedances due to parasitic capacitances in the actual circuit board transfer function. These parasitic capacitances effect the frequency response of the experimental results so that they do not match the simulation results. The preconditioner circuit is band limited by the parasitic capacitances found in the circuit board.

Equation (10) is the output equation for the circuit in Figure 2. This equation should correctly predict the output voltage of the preconditioner circuit. If the all the components of the preconditioner circuit are operating correctly, than the theoretical

results should correspond with both the simulated and experimental results. In Chapter III we will find out if all the results are in agreement with each other. Next, we will deduce the frequency in which the experimental results do not match up with simulation and theoretical results. Finally, we will determine the discrepancies between the experimental and simulation results and correct those discrepancies so that the results will be in accordance with design specifications.

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III. DATA ANALYSIS

Two experiments are used to analyze the response of the signal preconditioner circuit. In Figure 6, the preconditioner circuit board can be seen for Experiments 1 and 2. It includes the operational amplifier and the resistors that were used in both experiments. In the first experiment, a high voltage signal is connected to the voltage divider of the circuit to analyze the attenuation of an isolated higher voltage signal and the output signal from the amplifier. In the second experiment, a low voltage signal V_B is connected directly to the averaging circuit to analyze the frequency response of the amplifier. The experimental output values are compared to theoretical and simulated values for each respective experiment.

In the experimental results, calculations use measured values for resistances from a voltmeter.

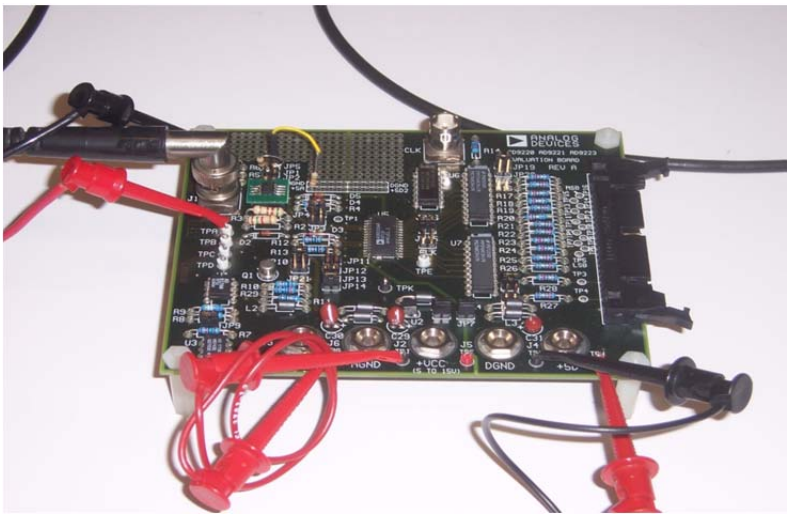

Figure 6. Circuit board for preconditioner testing.

All simulations results in this chapter were done using the PSPICE simulation program. All experimental measurements were done with the Tektronix TD 3014B, Four Channel Color Digital Phosphor Oscilloscope. All the oscilloscope images were transferred from the oscilloscope to the computer.

A. EXPERIMENT 1

1. Calculation of Mean Output Voltage and Peak-to-Peak Output Voltage

In the first experiment, a higher voltage signal is connected to the voltage divider of the circuit through an isolation transformer to analyze the attenuation of the signal and the output signal from the amplifier. From Figure 7, the voltage transformer and voltage divider can be seen from Experiment 1. The yellow insulators cover two 4.6 MΩ resistors, while the exposed resistor is 51 kΩ. The isolation transformer (left side of Figure 7) is necessary to break the ground loop that would otherwise occur between the sensed voltage and the power supply for the preconditioner circuit. In the target application, the preconditioner would be driven with a battery, and the input signal can be connected directly to the preconditioner input without an isolation transformer.

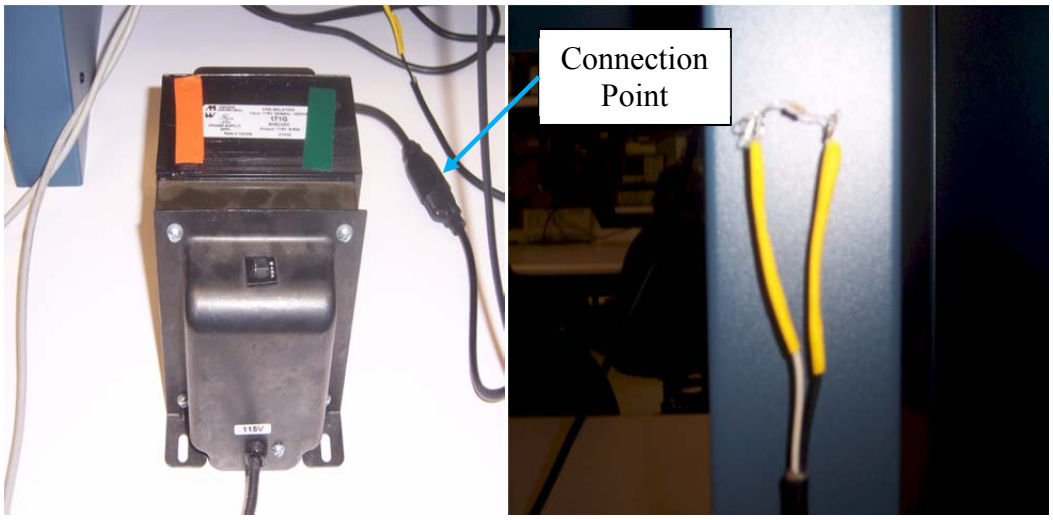

Figure 7. Isolation transformer and voltage divider circuit.

Recall the circuit in Figure 1 was used in the first experiment, and the circuit in Figure 2 is only used for analysis purposes. We next show how the experimental output values compared to theoretical and simulated values for the first experiment.

The voltage divider attenuated the input voltage of 115 volts rms, 162.7 volts peak, with a DC component of 0 volts to 0.868 volts peak, at node V_B according to

$$V_{Th} = V_{OC} = 162.7 \times \frac{51.15k}{4.837M + 4.695M + 51.15k} = 0.868\,\text{V}. \tag{11}$$

Note that the peak-to-peak voltage at V_B is 1.736 volts and that the DC component is 0 volts. At node V_A a DC component of 2.51 volts is added to the sinusoidal input wave while the peak-to-peak voltage is decreased from 1.736 volts to 0.86 volts because of the averaging circuit. The averaging circuit is comprised of the V_B and V_3 branches. The voltage is further increased to 2.80 volts DC with a peak-to-peak voltage of 0.97 volts at the output of the amplifier. The calculated mean output voltage and peak-to-peak output voltage at V_O match the values in Figures 8 and 9. In Figure 8, the input sinusoidal wave to the noninverting terminal of the amplifier is on channel 4, and the output sinusoidal wave of the amplifier is on channel 1. From Figure 9, the output sinusoidal wave can be seen from the simulation from PSPICE. The mean output voltage and peak-to-peak output voltage at V_O is slightly larger than the mean input voltage and peak-to-peak input voltage to the amplifier at node V_A because the gain of the noninverting amplifier is slightly greater than unity. In the following equations, V_{Th} and V_O are calculated for Experiment 1.

The first step is to calculate the open-circuit voltage using the peak voltage of the voltage source. The rms voltage of the voltage source is 120 volts but is attenuated by the isolation transformer to 115 volts. When the 115 volts rms voltage is converted to peak voltage, the value becomes 162.7 volts, which is used in Equation (11).

Once the open-circuit voltage is found, the short-circuit current is calculated by placing a short between V_B to V_2. The short-circuit current is calculated to be

$$i_{SC} = \frac{162.7}{4.837M + 4.695M} = 0.000017\,\text{A} \tag{12}$$

The short-circuit current is needed in order to calculate the Thévenin resistance. Thévenin resistance R_{Th} can easily be determined because it is the ratio of the open-circuit voltage to the short-circuit current. Now substituting the appropriate values into (10), we get

$$V_O = \left(\frac{R_F + R_G}{R_G}\right)\left[\frac{\left(\frac{V_3}{R_3} \pm \frac{V_{Th}(AC)}{R_{Th}+R_4}\right)}{\left(\frac{1}{R_{Th}+R_4}+\frac{1}{R_3}\right)}\right] = \left(\frac{4346+508.4}{4346}\right)\left[\frac{\left(\frac{5}{55.72k} \pm \frac{0.868}{50.87k+5107}\right)}{\left(\frac{1}{50.87k+5107}+\frac{1}{55.72k}\right)}\right].$$

$$= 3.28 \text{ max voltage}$$
$$2.31 \text{ min voltage}$$
$$\text{mean voltage of } 2.80\,\text{V}$$
$$0.97\,\text{Vpp} \qquad (13)$$

to compute the output voltage.

From (13), the mean voltage is 2.80 volts with a maximum value of 3.28 volts and a minimum value of 2.31 volts. The peak-to-peak output voltage is 0.97 volts. The results obtained from (13) are approximately equal to the output mean voltage and output peak-to-peak voltage seen in Figures 8 and 9. In Figure 8, the input sinusoidal wave to the noninverting terminal of the amplifier is on channel 4, and the output sinusoidal wave of the amplifier is on channel 1. From Figure 9, the output sinusoidal wave can be seen from the simulation from PSPICE. The output mean voltage and output peak-to-peak voltage are similar to the theoretical values calculated earlier in this chapter. The theoretical, simulation, and experimental values for Experiment 1 are tabulated in Table 1.

Table 1. Tabulated results for Experiment 1.

	Mean Voltage of Output	Peak-to-Peak Voltage of Output
Theoretical Values	2.80 V	0.97 V
Simulation Values	2.80 V	0.96 V
Experimental Values	2.80 V	0.96 V

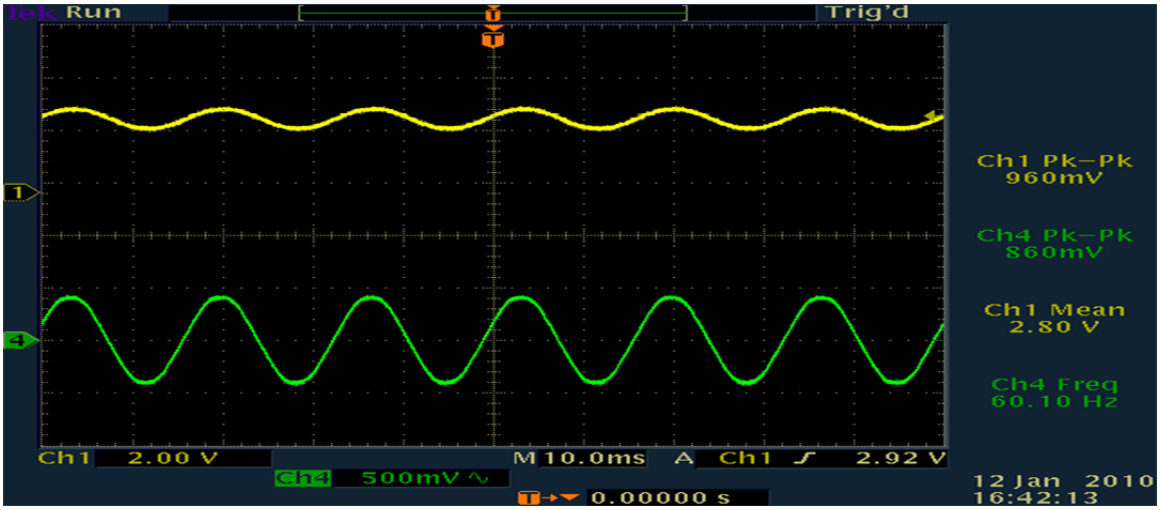

Figure 8. Measured signal at 60 Hz from the oscilloscope.

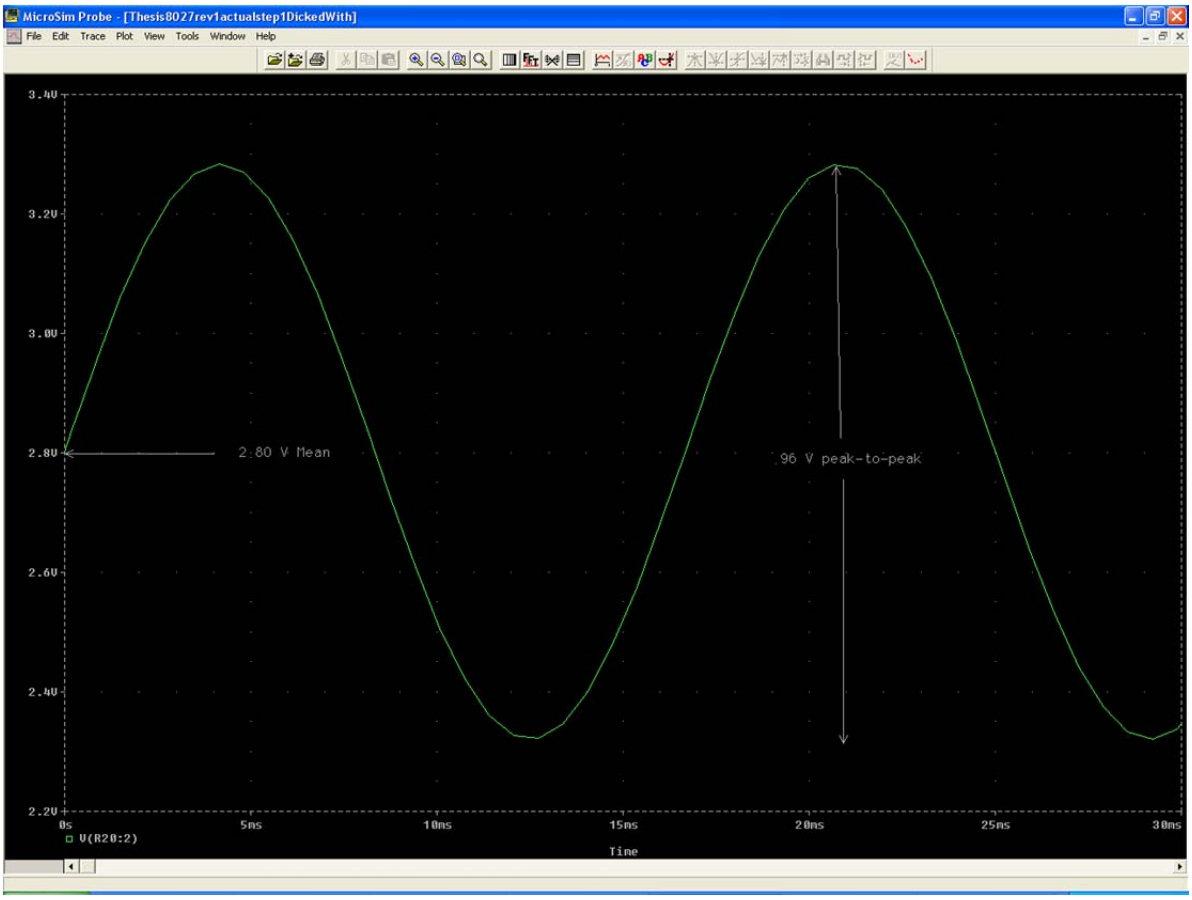

Figure 9. Simulation of signal at 60 Hz from PSPICE.

B. EXPERIMENT 2

1. Calculation of Mean Voltage and Peak-to-Peak Voltage

The preconditioner response to a variable frequency sine wave from a function generator was measured in Experiment 2. From Figure 10, the experimental circuit can be seen for Experiment 2.

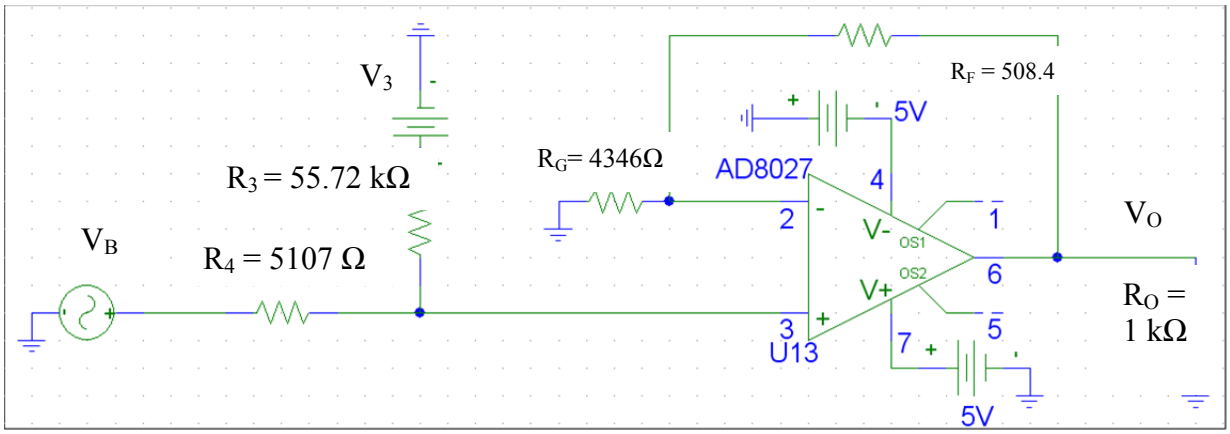

Figure 10. Circuit for Experiment 2.

Equation (10) was modified to fit the parameters of Experiment 2. There is not a R_{Th} variable, and V_{Th} was replaced with the voltage source V_B from Figure 10. The voltage V_B, the input sinusoidal wave, has a one volt peak-to-peak voltage swing with a one-half volt DC offset. These are arbitrary values but were used to demonstrate the behavior of the circuit. The output voltage V_O is determined from appropriate substitutions into (10) to obtain

$$V_O = \left(\frac{R_F + R_G}{R_G}\right)\left[\frac{\left(\frac{V_B(DC)}{R_4} + \frac{V_3}{R_3} \pm \frac{V_B(AC)}{R_4}\right)}{\left(\frac{1}{R_4} + \frac{1}{R_3}\right)}\right] = \left(\frac{4346 + 508.4}{4346}\right)\left[\frac{\left(\frac{0.5}{5107} + \frac{5}{55.72k} \pm \frac{0.5}{5107}\right)}{\left(\frac{1}{5107} + \frac{1}{55.72k}\right)}\right]. \quad (14)$$

$$= 1.49 \text{ max voltage}$$
$$0.47 \text{ min voltage}$$
$$\text{mean voltage of } 0.98\,\text{V}$$
$$1.02\,\text{Vpp}$$

From (14), the mean voltage is 0.98 volts with a maximum value of 1.49 volts and a minimum value of 0.47 volts. The peak-to-peak output voltage is 1.02 volts. The results from (14) are approximately equal to the mean output voltage and the peak-to-peak output voltage of Figure 11 from the oscilloscope and Figure 12 from the simulation. From the oscilloscope output shown in Figure 11 with channel 4 as the input and channel 1 as the output, the experimental mean output voltage is 0.968 volts, and the experimental peak-to-peak output voltage is 1.04 volts. From the PSPICE simulation in Figure 12, the sinusoidal wave has a mean output voltage is 0.968 volts, and the peak-to-peak output voltage is 1.02 volts. The theoretical, simulation, and experimental values from Experiment 2 are tabulated in Table 2.

Table 2. Tabulated results for Experiment 2.

	Mean Voltage of Output	Peak-to-Peak Voltage of Output
Theoretical Values	0.98 V	1.02 V
Simulation Values	968 mV	1.02 V
Experimental Values	968 mV	1.04 V

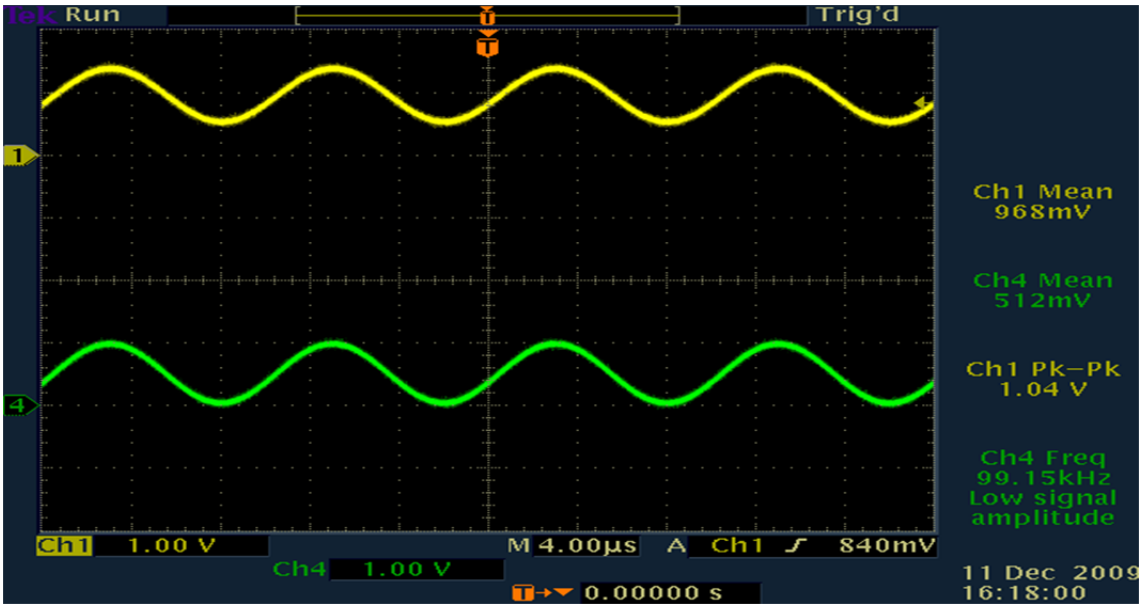

Figure 11. Signal frequency output of 100 kHz.

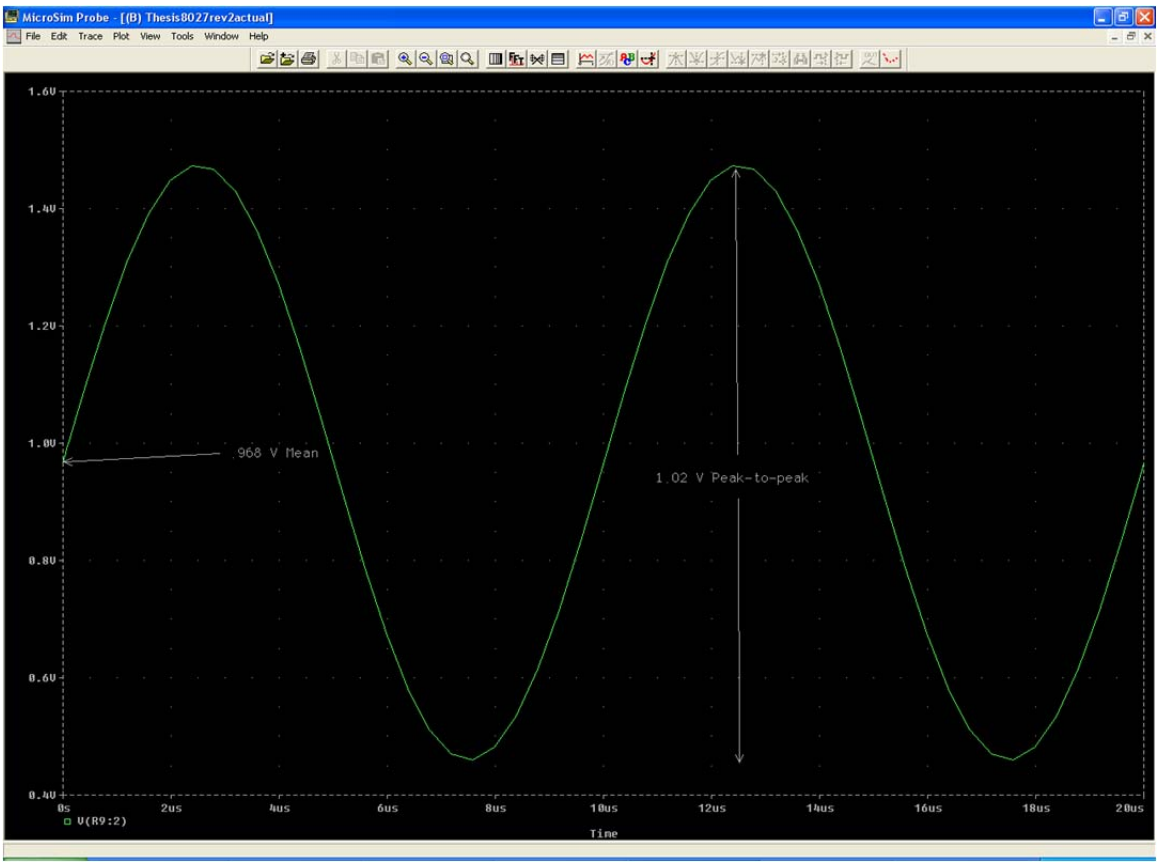

Figure 12. Signal frequency of 100 kHz.

2. Calculation of 3 dB Point

The 3 dB frequency occurs at the point where the peak-to-peak output voltage is 0.707 times the peak-to-peak input voltage. In Experiment 2, from

$$\begin{aligned} 3\text{ dB Voltage} &= .707 \times \text{Peak-to-Peak Output Voltage} \\ &= .707 \times 1.02 = 0.721\,\text{V} \end{aligned} \tag{15}$$

the 3 dB voltage is approximately 0.721 V.

The simulation software and the spectrum analyzer have considerably different results for the 3 dB frequency. The 3 dB frequency from the simulation is at 66.578 MHz, which is significantly larger than the 3 dB frequency of 3.69 MHz from the spectrum analyzer. From Figures 13 and 14, the frequency sweeps can be seen from the spectrum analyzer and simulation results, respectively [5]. To measure the frequency sweep of the spectrum analyzer, we connected the spectrum analyzer to the noninverting

terminal of an AD8027 amplifier, AIN, and to the output of the AD8027 amplifier, test point TPA. Those two points measured the frequency response of the AD8027 amplifier. From Figure 13, we made a marker at the lowest frequency after the spike in the lower frequencies of the figure. This spike is caused the by DC component of the lower frequencies. We then put another marker 3 dB down on the curve. Finally, we turned the markers off to obtain the absolute frequency at the 3 dB point, 3.69 MHz, and the absolute power at that point, -0.69 dBm.

The AD8027 Analog Devices specification sheet gives a 3 dB bandwidth range which is closer to the 3 dB frequency of 66.578 MHz from the simulation software. The specification sheet gives a 3 dB bandwidth range of 203–2 MHz for an input voltage of two volts peak-to-peak with an amplifier gain of one. Additionally, the specification sheet gives a one fifth volt peak-to-peak input voltage with an amplifier gain of one a 3 dB bandwidth range from 1381–90 MHz. The input voltage for Experiment 2 was one volt peak-to-peak with an amplifier gain of approximately one, so the expected 3 dB frequency would be somewhere in between those ranges. The 3 dB frequency of 66.578 MHz from the simulation software falls nicely in between those ranges and is therefore realistic [6].

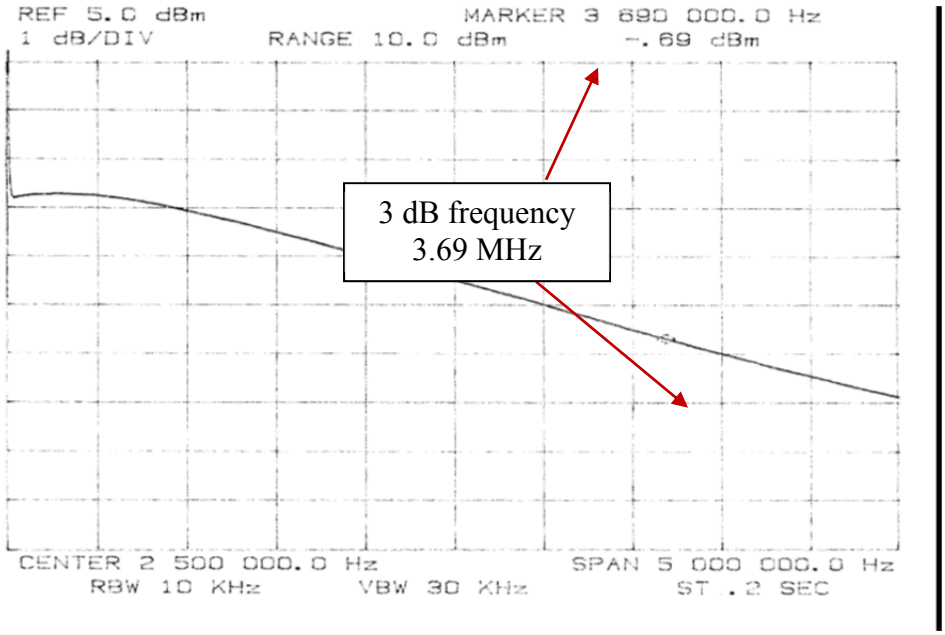

Figure 13. Frequency sweep on spectrum analyzer.

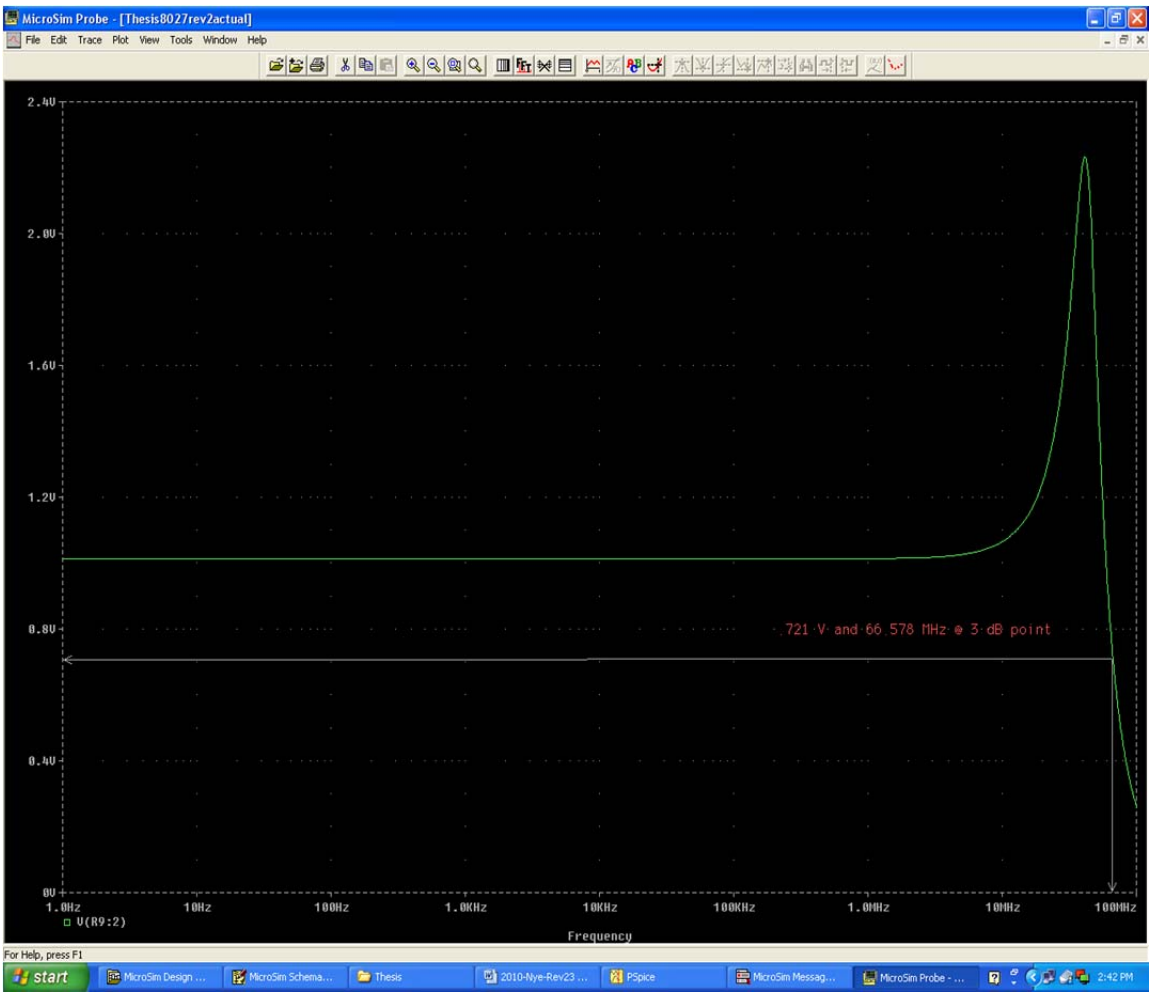

Figure 14. Frequency sweep in PSPICE.

The peak-to-peak output voltage at the 3 dB frequency is attenuated to 0.707 times the pass band peak-to-peak output voltage at 100 kHz. From the simulation results, in Figure 15, the input waveform can be seen for the circuit in Figure 10. From Figures 12 and 16, the output waveforms can be seen at 100 kHz and 66.578 MHz, respectively. From Figure 16 it can be seen that the peak-to-peak output voltage at the 3 dB frequency, 66.578 MHz, has attenuated to approximately 0.707 times the peak-to-peak output voltage from Figure 11. The peak-to-peak output voltage decreased from 1.02 volts to approximately 0.721 volts. The expected peak-to-peak output voltage at the 3 dB frequency was 0.721 volts from (15).

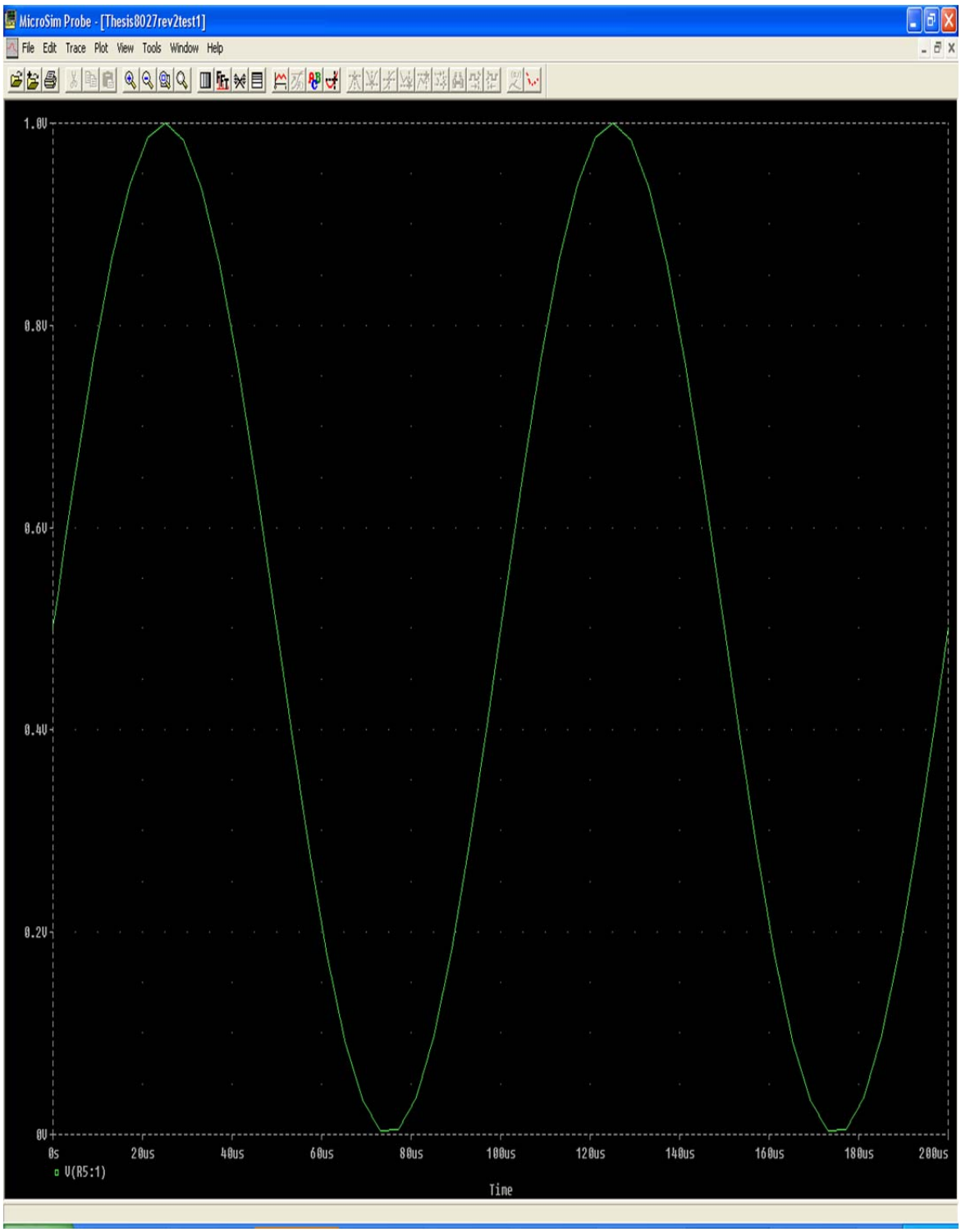

Figure 15. Signal frequency input of 100 kHz.

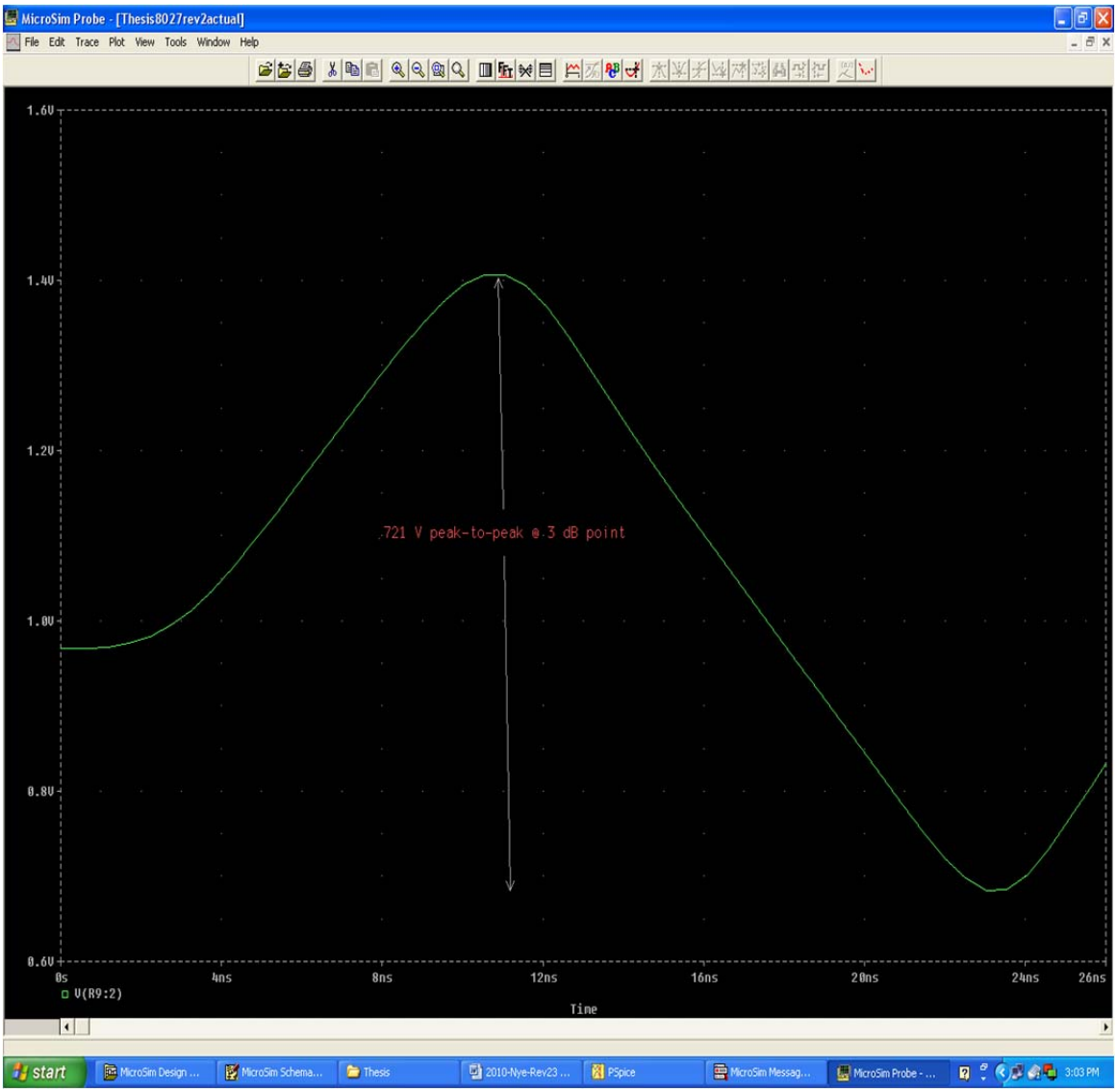

Figure 16. Signal frequency output of 66.578 MHz.

From Figures 17 and 18, the measured output waveforms can be seen at 100 kHz and 3.69 MHz, the 3 dB frequency from the Spectrum Analyzer, on channel 1 in each respective figure. The input sinusoidal wave on channel 4 in each respective figure is a one volt peak-to-peak voltage swing with a one half volt DC offset. Just as with the plots from the simulation software, there is a decrease in peak-to-peak output voltage to approximately 0.707 times the pass band peak-to-peak output voltage. The peak-to-peak output voltage decreased from 1.04 volts to 0.741 volts.

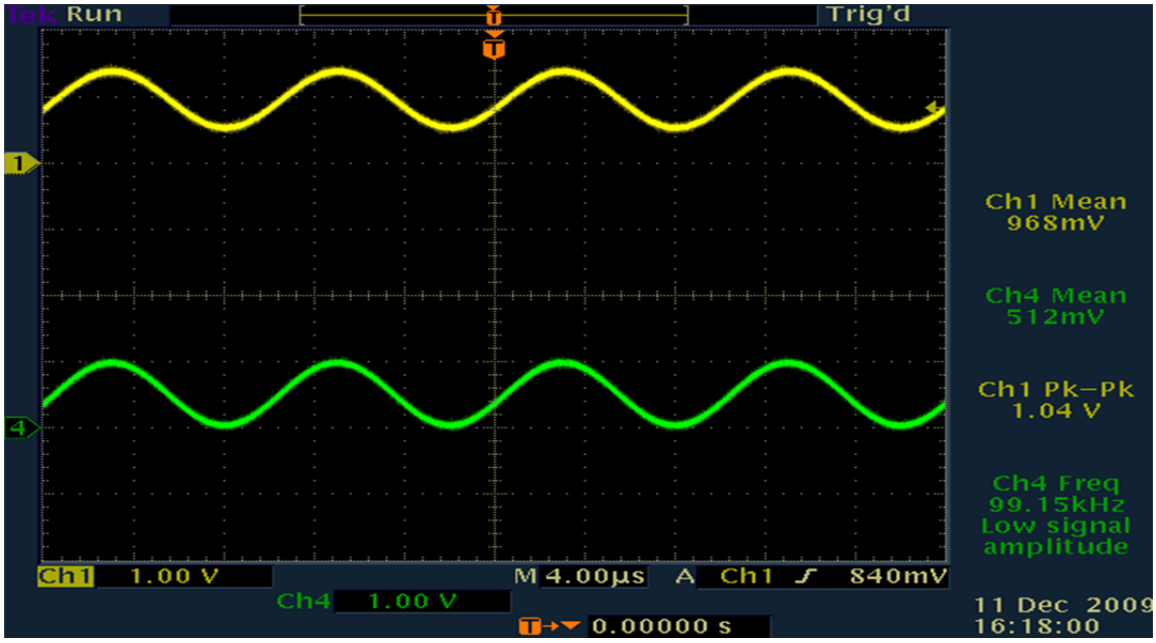

Figure 17. Signal frequency of 100 kHz.

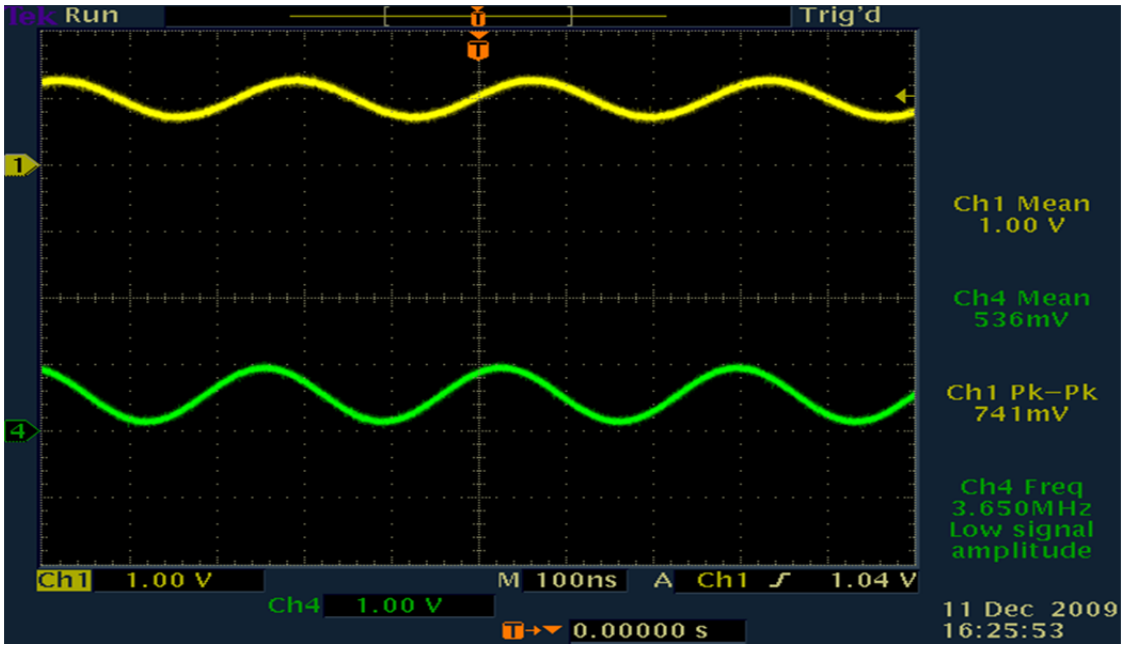

Figure 18. Signal frequency of 3.69 MHz.

From Table 2, the natural attenuation can be seen in peak-to-peak output voltage for the circuit in Figure 10 from experimental data. This circuit behaves as a low-pass

filter with a bandwidth of 3.69 MHz. After the 3 dB frequency, the peak-to-peak output voltage decays linearly at 20 dB per decade in frequency [5].

Table 3. Frequencies effect on output waveform.

Input Frequency	Mean Voltage of Output	Peak-to-Peak Voltage of Output
10 kHz	962 mV	1.04 V
500 kHz	978 mV	1.00 V
1 MHz	1.02 V	1.00 V
1.5 MHz	954 mV	960 mV
2.0 MHz	996 mV	923 mV
2.5 MHz	1.01 V	860 mV
3.0 MHz	1.00 V	820 mV
3.5 MHz	998 mV	742 mV
4.0 MHz	1.00 V	740 mV
4.5 MHz	999 mV	681 mV
5.0 MHz	985 mV	684 mV

3. Analyzing the Differences between the Experimental and Simulated Frequency Responses

The difference between the experimental and simulated frequency responses was because the simulation circuit model did not account for the parasitic capacitances of the actual circuit board. Whereas the operational amplifier has a bandwidth of about 190 MHz, the parasitic capacitances in the circuit greatly reduce the bandwidth. This is a useful result because it identifies how the circuit bandwidth can be improved in the future. A parasitic capacitance was created between the ground plane and both operational amplifier terminals. Both elements form a capacitor because they are insulated from one another, carrying a charge, and have a voltage potential between them.

From Figure 19, the circuit can be seen with the two parasitic capacitances between the ground plane and both operational amplifier terminals. The parasitic capacitances are labeled C_{p1} and C_{p2} in Figure 19.

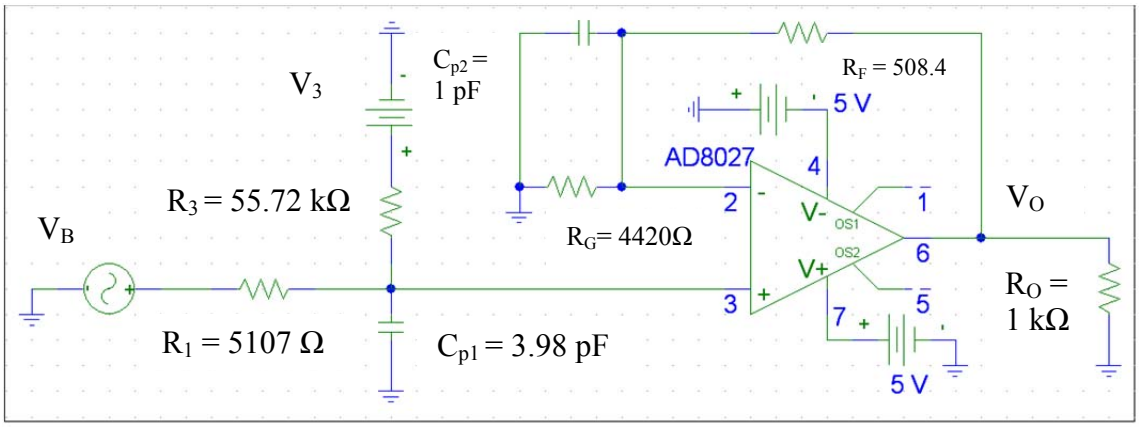

Figure 19. Circuit for Experiment 2 with parasitic capacitances.

From the simulation in Figure 20, it can be seen that the 3 dB point was reduced to 3.69 MHz, which is the same as the experimental frequency response in Figure 14. The transfer function for the circuit in Figure 19 is

$$V_O = \left(\frac{R_G + R_F\left(1 + sC_{p2}R_G\right)}{R_G} \right) \left[\frac{\left(\frac{V_B}{R_4} + \frac{V_3}{R_3} \right)}{\left(sC_{p1} + \frac{1}{R_3} + \frac{1}{R_4} \right)} \right]. \tag{16}$$

The transfer function in (16) is plotted in Figure 21. From Figure 21, it can be seen that the 3 dB bandwidth of 3.69 MHz matches the value in Figure 20. The calculated value of the voltage at the 3 dB frequency is

$$V_O = \left(\frac{4420\,\Omega + 508.4\,\Omega\left(1 + 2\pi\left(3.69\,\text{MHz}\right)\left(1\,\text{pF}\right)\left(4420\,\Omega\right)\right)}{4420\,\Omega} \right) \times \left[\frac{\left(\frac{1\,\text{V}}{5107\,\Omega} + \frac{0}{55720\,\Omega} \right)}{\left(2\pi\left(3.69\,\text{MHz}\right)\left(3.98\,\text{pF}\right) + \frac{1}{55720\,\Omega} + \frac{1}{5107\,\Omega} \right)} \right] = 0.721\,\text{V}. \tag{17}$$

It can be seen that this result matches those in Figures 13 and 20 [7].

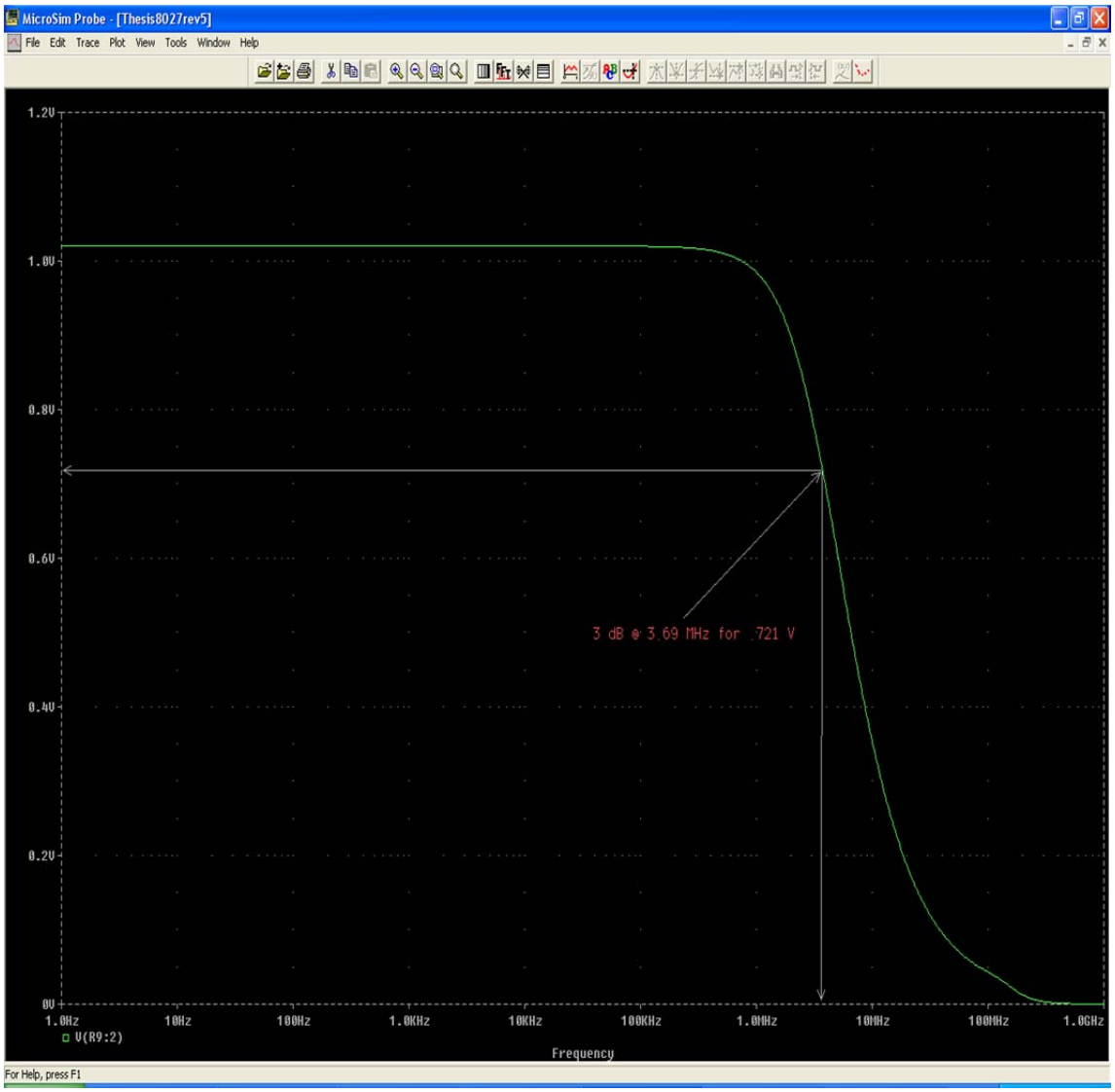

Figure 20. Simulation of circuit for Experiment 2 with parasitic capacitances.

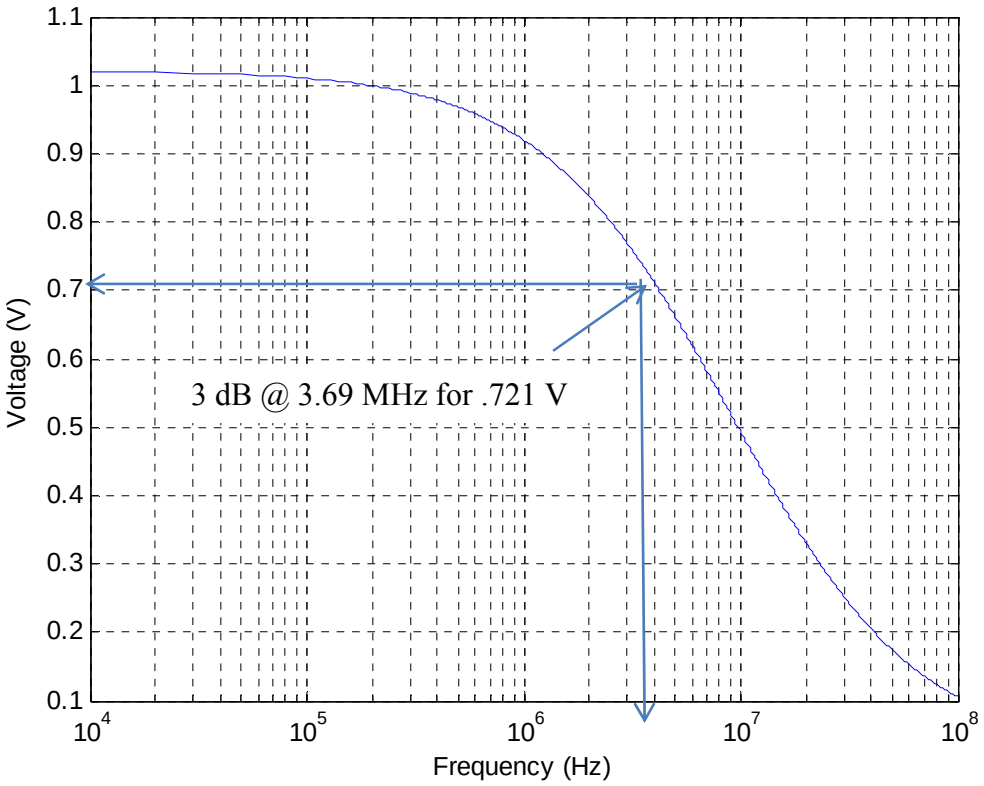

Figure 21. Plot of simulation of circuit for Experiment 2 with parasitic capacitancs.

In this chapter, we compared the experimental output values to the theoretical and simulated values for each respective experiment. In Chapter IV, we will go over both experiments in detail.

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IV. RESEARCH EXPERIMENTS

Two experiments were designed to analyze the response of the signal preconditioner circuit. These two experiments test the operation of every component of the signal preconditioner circuit, which includes the voltage divider, passive averaging circuit, and operational amplifier. In the first experiment, a high voltage signal, a 120 volts rms sine wave at 60 Hz from the bench electrical outlet, is connected to the voltage divider of the circuit with an isolation transformer to analyze the attenuation of the signal and the output signal from the amplifier. In the second experiment, a low voltage signal, a one volt peak-to-peak sine wave with a mean value of 500 mV, is connected directly to the averaging circuit to analyze the effect of the frequency response of the amplifier. The frequency range tested for the first experiment is from 10 kHz to 5 MHz.

In Chapter III the expected results from both of the experiments and simulations should correspond to the theoretical computations for each respective experiment. These theoretical computations are based on circuit analysis performed in Chapter II.

In this chapter both experiments are described in detail. Both experiments are broken up into four sections which are titled: purpose, equipment, set-up, and procedure. In Experiment 1 the voltage divider was utilized to determine the attenuation of the signal. Additionally, the output of circuit is analyzed to determine its agreement with both theoretical and simulated values. In Experiment 2 the frequency response of the circuit was analyzed, and the 3 dB frequency was determined using the spectrum analyzer. The experimental and simulation frequency responses were different due to parasitic capacitances in the experimental circuit board. The preconditioner circuit was band limited by the parasitic capacitances found in the circuit board. We performed a simulation with parasitic capacitances added to the circuit.

If the experimental results match the theoretical and simulation results, then the signal preconditioner circuit has been properly designed and built to function within specifications. A properly functioning signal preconditioner circuit has many applications in electronics. Voltages up to 10,000 volts or higher can be attenuated and measured to provide control feedback for many applications like medium voltage generators or

pulsedpower systems. The conditioned signal can be inputted to analog control circuits or analog-to-digital converters to ensure that the equipment is operating within specifications.

A. EXPERIMENT 1

1. Purpose

A high voltage signal is connected to the voltage divider of the circuit to analyze the attenuation of the signal and the output signal from the amplifier.

2. Equipment

a. Agilent E3631A, triple output DC power supply
b. Tektronix TDS 3014B, four channel color digital phosphor oscilloscope
c. Analog Devices AD9220 evaluation board
d. Hammond Manufacturing 115 volt isolation transformer
e. T-connector
f. Voltage divider branch

3. Setup

a. Plug T-connector into oscilloscope.

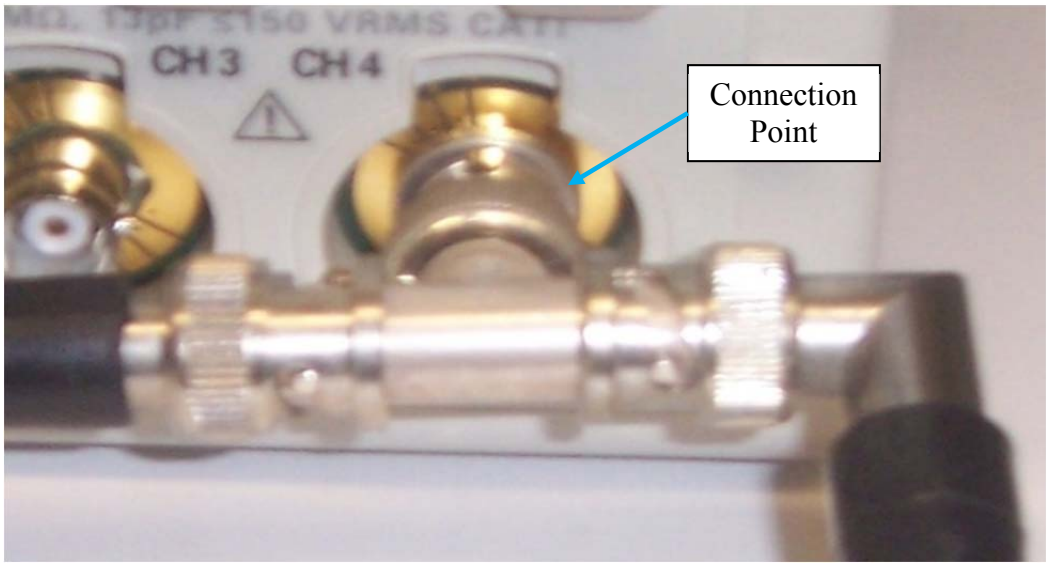

Figure 22. T-connector plugged into oscilloscope.

b. Plug the isolation transformer into a 120 volt outlet.

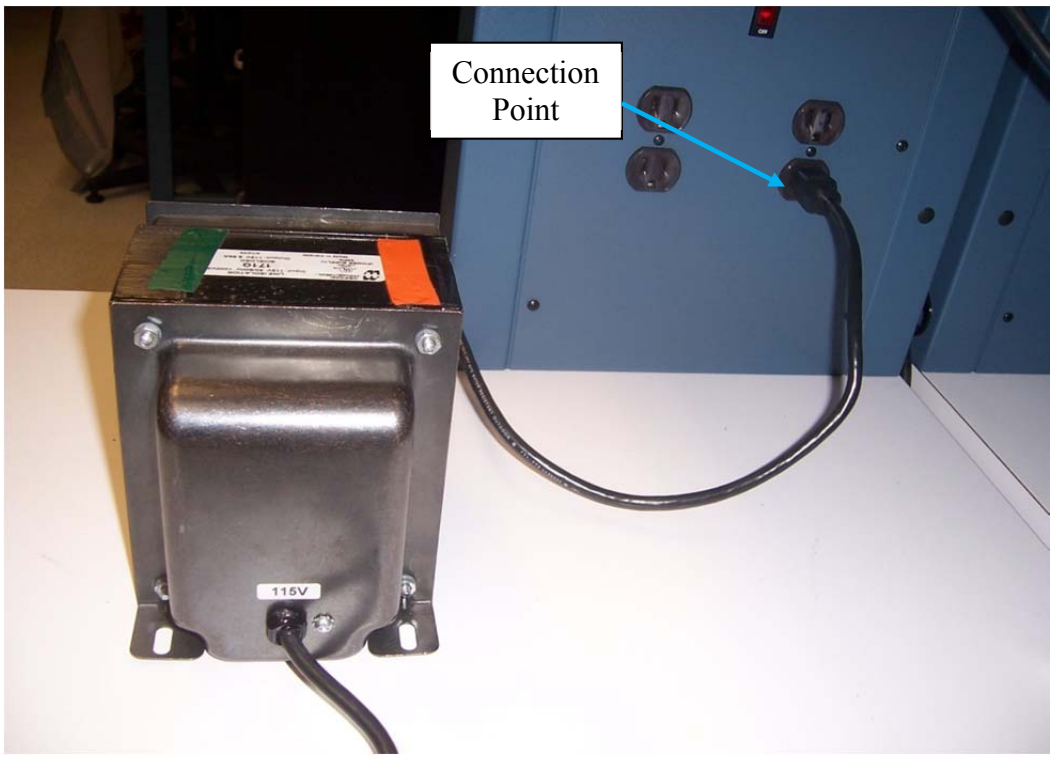

Figure 23. Isolation transformer plugged into wall outlet.

c. Plug the voltage divider branch to the isolation transformer.

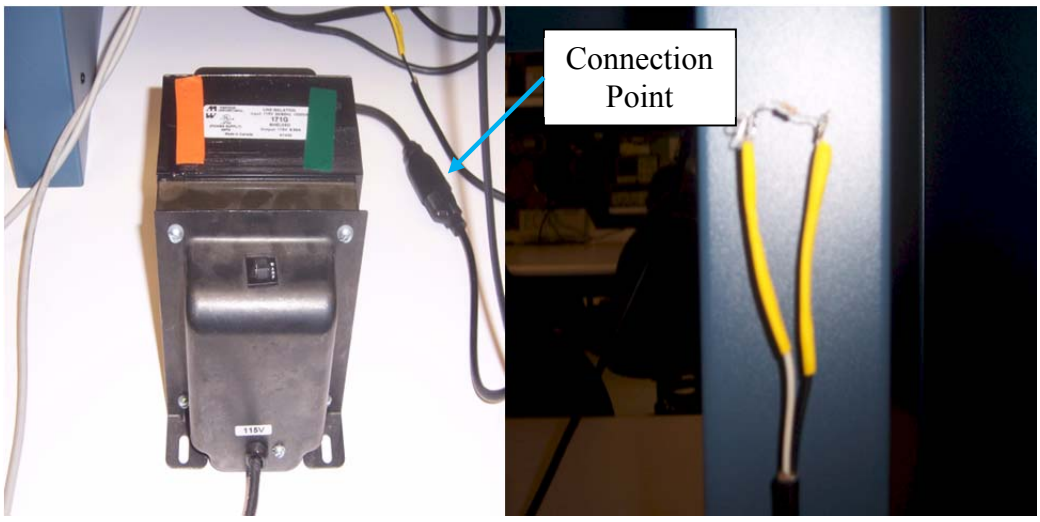

Figure 24. Voltage divider branch plugged into isolation transformer.

d. Connect the voltage divider branch to the oscilloscope via one end of the T-connector.

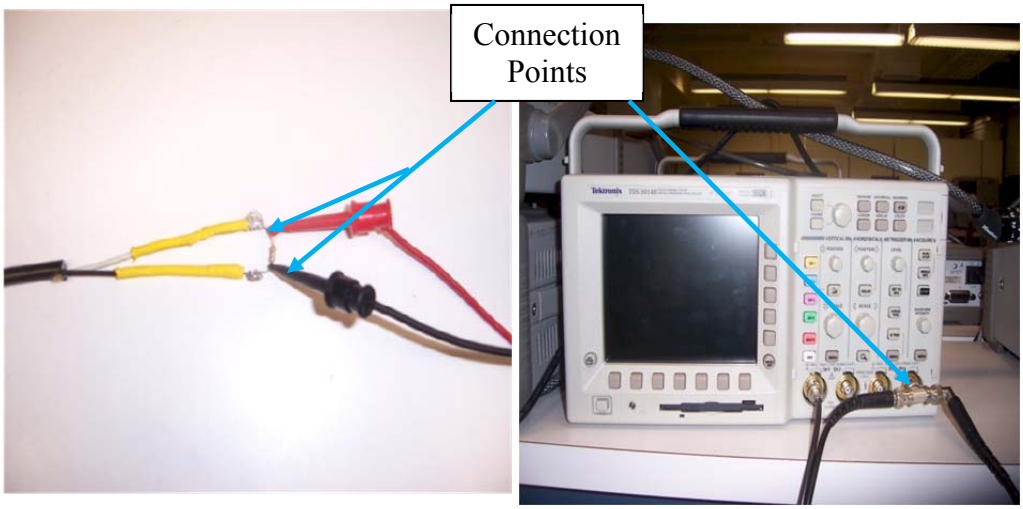

Figure 25. Voltage divider branch connected to oscilloscope via T-connector.

e. Connect the input to the evaluation board, AIN, to the oscilloscope via the other end of the T-connector.

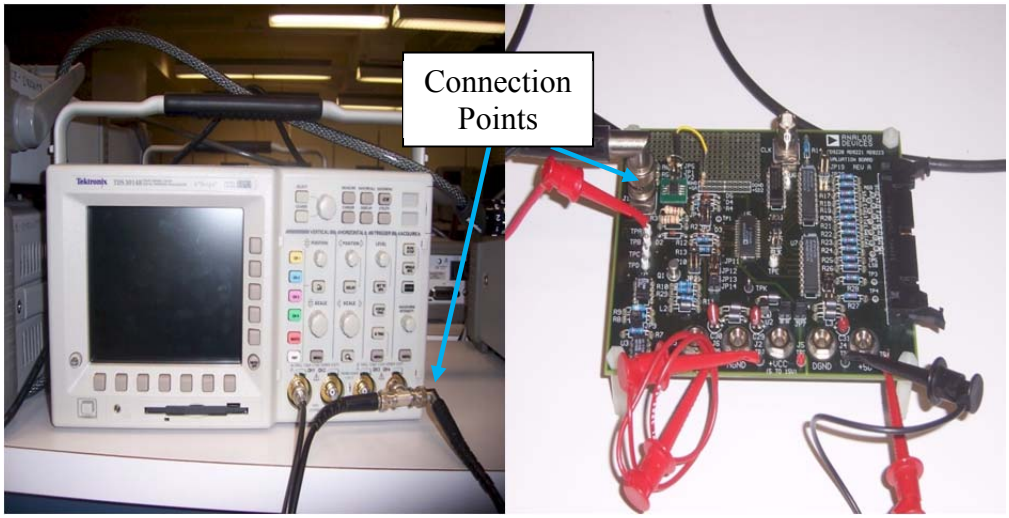

Figure 26. Oscilloscope via T-connector connected to evaluation board.

f. Connect the power supply to the evaluation board. Use the points +5D and DGND on the evaluation board. The power supply will provide the 5 volts DC component to the V_3 branch for the averaging circuit.

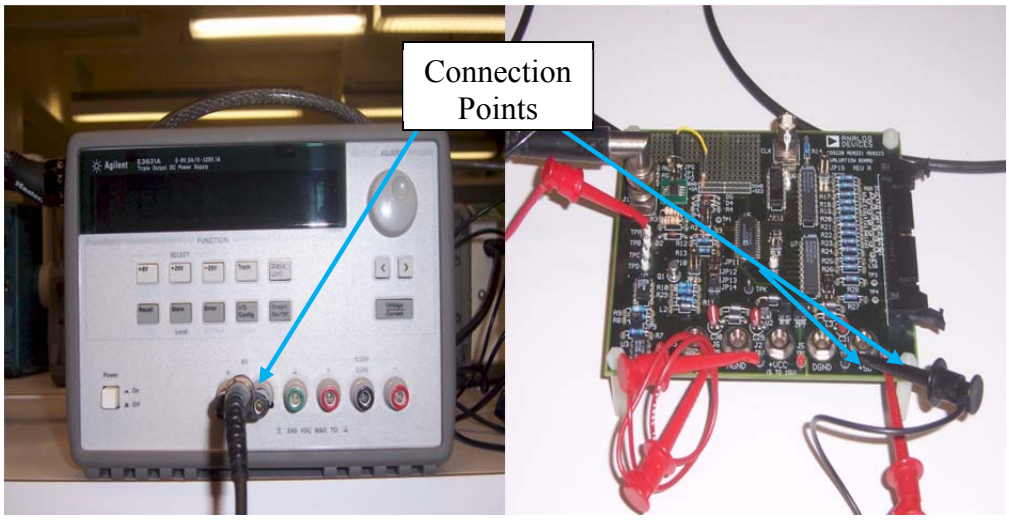

Figure 27. Power supply connected to evaluation board.

g. Connect the output of the evaluation board to the oscilloscope. Use the points TPA and TPL on the evaluation board.

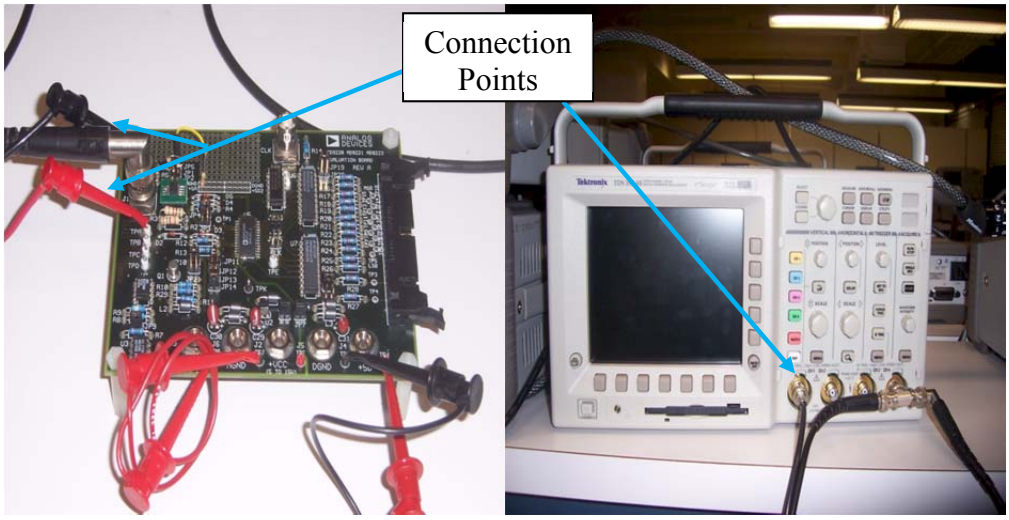

Figure 28. Evaluation board connected to oscilloscope.

4. Procedure

a. Turn on the power to the oscilloscope, power supply, and function generator.
b. Set the power supply to +5 volts.
c. Observe 60 Hz input and output waveforms on oscilloscope. Copy a picture onto a disk from the oscilloscope.
d. Simulate circuit from Figure 2 on PSPICE and compare results with experimental data and theoretical computations.

B. EXPERIMENT 2

1. Purpose

In this experiment, a low voltage signal at a range of frequencies was inputted into the circuit to analyze the frequency response of the circuit. From analysis of the frequency response of the circuit, the 3 dB frequency, where the peak-to-peak output voltage is .707 times the peak-to-peak input voltage, can be determined from the output.

2. Equipment

a. Agilent E3631A, triple output DC power supply
b. Tektronix TDS 3014B, four channel color digital phosphor oscilloscope
c. Analog Devices AD9220 evaluation board
d. Hammond Manufacturing 115 volt isolation transformer
e. T-connector
f. Voltage divider branch

3. Setup

a. Plug T-Connector into oscilloscope.

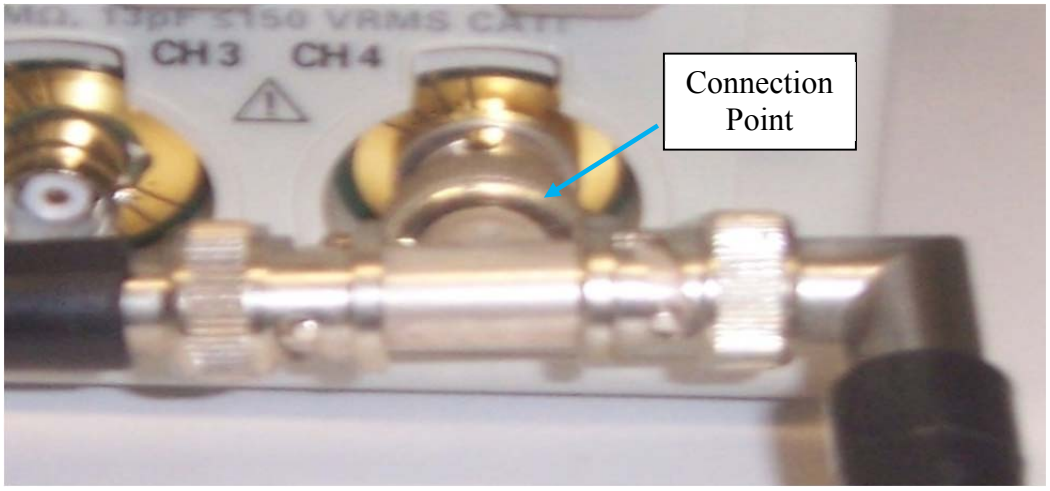

Figure 29. T-connector plugged into oscilloscope.

b. Connect the function generator to the oscilloscope via one end of the T-connector.

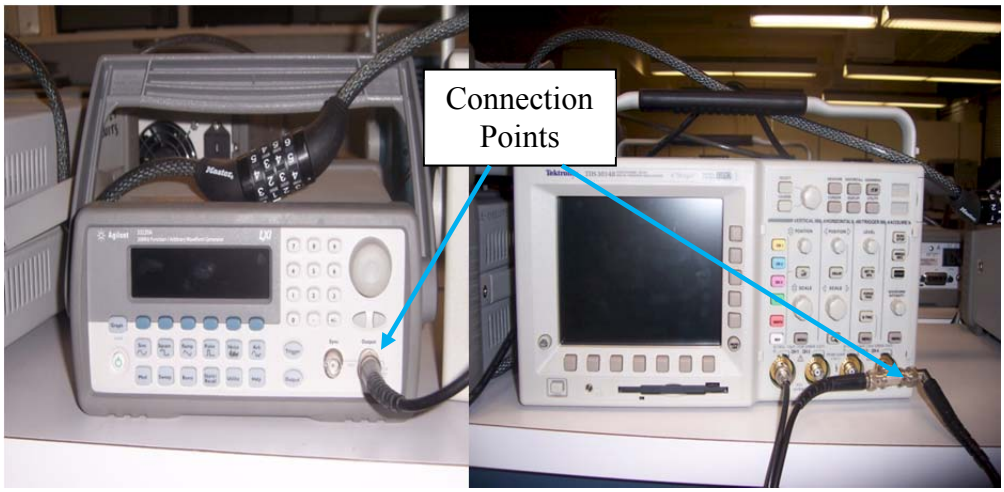

Figure 30. Function generator connected to oscilloscope via T-connector.

c. Connect the input to the evaluation board, AIN, to the oscilloscope via the other end of the T-connector.

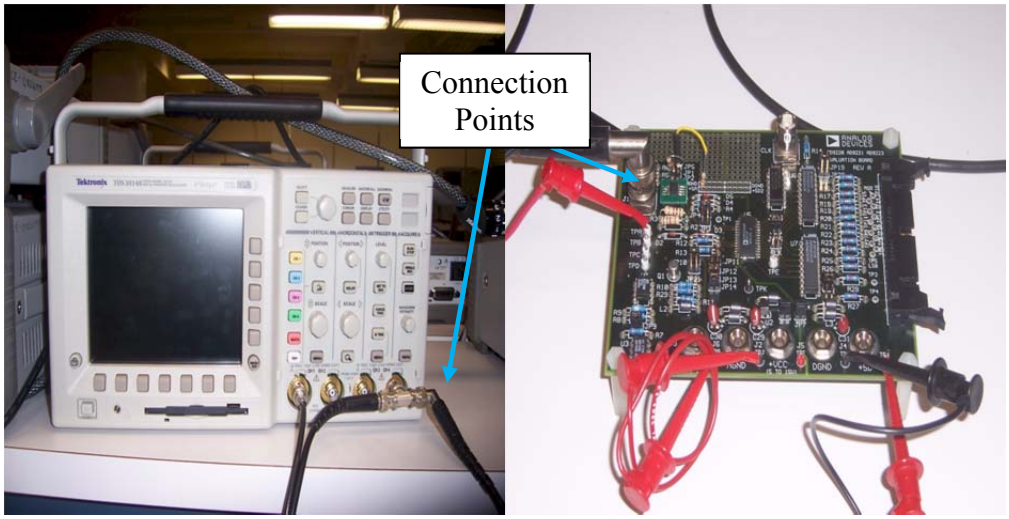

Figure 31. Oscilloscope via T-connector connected to evaluation board.

d. Connect the power supply to the evaluation board. Use the points +5D and DGND on the evaluation board. The power supply will provide the 5 volts DC component to the V_3 branch for the averaging circuit.

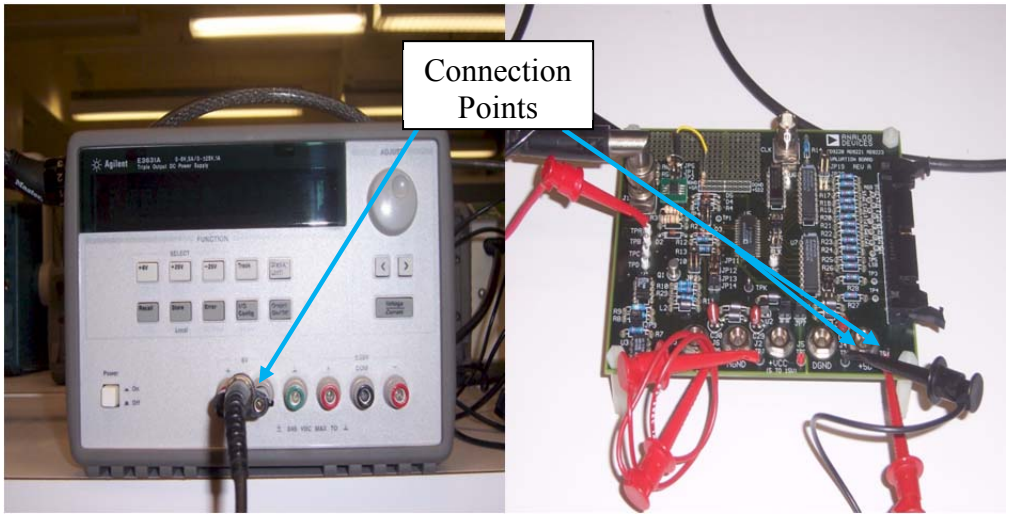

Figure 32. Power supply connected to evaluation board.

e. Connect the output of the evaluation board to the oscilloscope. Use the points TPA and TPL on the evaluation board.

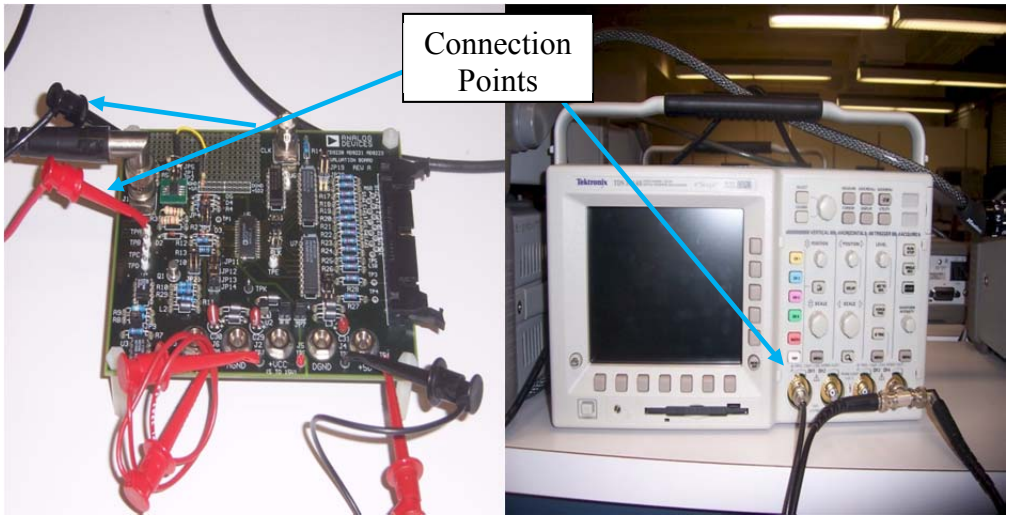

Figure 33. Evaluation board connected to oscilloscope.

4. Procedure

a. Turn on the power to the oscilloscope, power supply, and function generator.

b. Set the power supply to +5 volts.

c. Set the function generator to output a 1 volt peak-to-peak sine wave with a mean value of 500 mV. The signal will have a mean value of 500 mV by giving it a DC offset of 500 mV.

d. Step through the following frequencies:
10 kHz, 100 kHz, 500 kHz, 1 MHz, 1.5 MHz, 2 MHz, 2.5 MHz,
3 MHz, 3.5 MHz, 3.69 MHz, 4 MHz, 4.5 MHz, 5 MHz
Copy a picture from the oscilloscope onto a disk for each frequency.

e. Connect the output of the evaluation board to the spectrum analyzer. Observe the frequency response of the circuit on the screen of the spectrum analyzer. Connect the spectrum analyzer to the noninverting terminal of an AD8027 amplifier, AIN, and to the output of the AD8027 amplifier, test point TPA. Those two points allow the frequency response of the AD8027 amplifier to be measured. Make a marker at the lowest frequency after the spike in the lower frequencies

of the figure. This spike is caused the by the DC component of the lower frequencies. Then put another marker 3 dB down on the curve and turn the markers off so that it gives an absolute frequency at the 3 dB point and the absolute power at that point.

Figure 34. Spectrum analyzer.

f. Simulate circuit from Figure 10 on PSPICE and compare results with experimental data and theoretical computation. How is the simulated frequency response different from the experimental frequency response?

g. Simulate circuits from Figure 19 in PSPICE and compare results with experimental data and theoretical computation. How is this simulation's frequency response compared to the experimental frequency response? Why are it the same or different to the experimental frequency response?

In this chapter, the two experiments were explained in detail. Both experiments were necessary to analyze the response of the circuit in Figure 1. In the next chapter, we present the conclusions from the experiments and point out further work recommendations that would expand upon the results of this thesis.

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V. CONCLUSIONS/FURTHER RESEARCH

A. CONCLUSIONS

For both experiments, the experimental results closely match both theoretical and simulation results, except in frequency response. The mean output voltage and the peak-to-peak output voltage are approximately equal in theoretical computations, simulations of the circuit, and experimental data. The experimental 3 dB point was significantly smaller than that of the simulation's frequency response. This is due to parasitic capacitances in the experimental circuit board. This means that the signal preconditioner circuit was correctly modeled and inefficiencies were determined. The circuit board's frequency response was band limited by the parasitic capacitances in the circuit board. If the circuit board was built to reduce the parasitic capacitances, the circuit board would operate with higher bandwidth. The preconditioner circuit would then be designed to operate in a wider dynamic range of frequencies.

B. FURTHER WORK

We designed, built, and analyzed a signal preconditioner circuit. The circuit frequency response could be improved with correctly placed compensatory capacitors to negate the effects of parasitic capacitances, as suggested in [7]. Two compensatory capacitors would have to be added to the preconditioner circuit. The capacitor would be placed in parallel with R_F to cancel the effect of C_{p2} and then feedback factor will look purely resistive. Another capacitor would be placed in parallel to R_4 to compensate for the effects of the parasitic capacitance C_{p1} and then $V_P \simeq V_B$. A properly conditioned signal from this signal preconditioner circuit can be inputted to analog control circuits or analog-to-digital converters to ensure the equipment is operating within specifications. If a conditioned signal detects that the equipment is not operating within specifications, a protocol must be put into place to automatically adjust the equipment. For further research, circuitry or a program could be designed to place the equipment back to operating within specifications. This circuitry could to placed locally or remotely to the equipment. If the circuitry is placed remotely, then it would have to be connected to the operating equipment by a computer network, such as a Local Area Network.

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APPENDIX: DATASHEETS

ANALOG DEVICES

Low Distortion, High Speed Rail-to-Rail Input/Output Amplifiers

AD8027/AD8028

FEATURES

High speed
- **190 MHz, –3 dB bandwidth (G = +1)**
- **100 V/µs slew rate**

Low distortion
- **120 dBc @ 1 MHz SFDR**
- **80 dBc @ 5 MHz SFDR**

Selectable input crossover threshold

Low noise
- **4.3 nV/√Hz**
- **1.6 pA/√Hz**

Low offset voltage: 900 µV max

Low power: 6.5 mA/amplifier supply current

Power-down mode

No phase reversal: V_{IN} > |V_S| + 200 mV

Wide supply range: 2.7 V to 12 V

Small packaging: SOIC-8, SOT-23-6, MSOP-10

APPLICATIONS

Filters

ADC drivers

Level shifting

Buffering

Professional video

Low voltage instrumentation

GENERAL DESCRIPTION

The AD8027/AD8028[1] is a high speed amplifier with rail-to-rail input and output that operates on low supply voltages and is optimized for high performance and wide dynamic signal range. The AD8027/AD8028 has low noise (4.3 nV/√Hz, 1.6 pA/√Hz) and low distortion (120 dBc @ 1 MHz). In applications that use a fraction of or the entire input dynamic range and require low distortion, the AD8027/AD8028 is an ideal choice.

Many rail-to-rail input amplifiers have an input stage that switches from one differential pair to another as the input signal crosses a threshold voltage, which causes distortion. The AD8027/AD8028 has a unique feature that allows the user to select the input crossover threshold voltage through the SELECT pin. This feature controls the voltage at which the complementary transistor input pairs switch. The AD8027/AD8028 also has intrinsically low crossover distortion.

CONNECTION DIAGRAMS

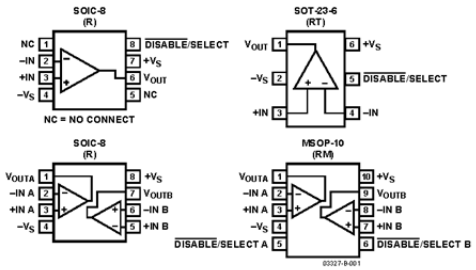

Figure 1. Connection Diagrams (Top View)

With its wide supply voltage range (2.7 V to 12 V) and wide bandwidth (190 MHz), the AD8027/AD8028 amplifier is designed to work in a variety of applications where speed and performance are needed on low supply voltages. The high performance of the AD8027/AD8028 is achieved with a quiescent current of only 6.5 mA/amplifier typical. The AD8027/AD8028 has a shut down mode that is controlled via the SELECT pin.

The AD8027/AD8028 is available in SOIC-8, MSOP-10, and SOT-23-6 packages. They are rated to work over the industrial temperature range of –40°C to +125°C.

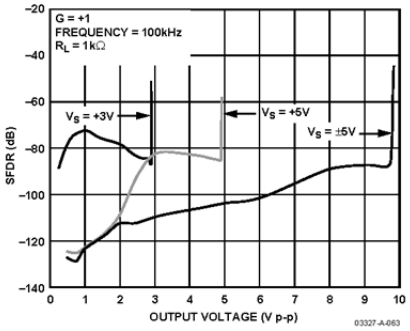

Figure 2. SFDR vs. Output Amplitude

[1]Protected by U.S. patent numbers 6,486,737B1; 6,518,842B1

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TABLE OF CONTENTS

REVISION HISTORY

Revision B:
10/03—Data Sheet changed from Rev. A to Rev. B

Changes to Figure 1 ... 1

Revision A:
8/03—Data Sheet changed from Rev. 0 to Rev. A

Addition of AD8028 ... Universal
Changes to GENERAL DESCRIPTION ... 1
Changes to Figures 1, 3, 4, 8, 13, 15, 17 ... 1, 6, 7, 8, 9
Changes to Figures 58, 60 ... 18, 20
Changes to SPECIFICATIONS ... 3
Updated OUTLINE DIMENSIONS ... 22
Updated ORDERING GUIDE ... 23

Revision 0: Initial Version

SPECIFICATIONS

Table 1. V_S = ±5 V (@ T_A = 25°C, R_L = 1 kΩ to midsupply, G = +1, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	138	190		MHz
	G = +1, V_O = 2 V p-p	20	32		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		16		MHz
Slew Rate	G = +1, V_O = 2 V Step/G = −1, V_O = 2 V Step		90/100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		35		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		120		dBc
	f_C = 5 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		80		dBc
Input Voltage Noise	f = 100 kHz		4.3		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.1		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.2		Degree
Crosstalk, Output to Output	G = +1, R_L =100 Ω, V_{OUT} = 2 V p-p, V_S = ±5 V @ 1 MHz		−93		dB
DC PERFORMANCE					
Input Offset Voltage	SELECT = Tri-State or Open, PNP Active		200	800	µV
	SELECT = High NPN Active		240	900	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.50		µV/°C
Input Bias Current[1]	V_{CM} = 0 V, NPN Active		4	6	µA
	T_{MIN} to T_{MAX}		4		µA
Input Bias Current[1]	V_{CM} = 0 V, PNP Active		−8	−11	µA
	T_{MIN} to T_{MAX}		−8		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_O = ±2.5 V	100	110		dB
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			−5.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	90	110		dB
SELECT PIN					
Crossover Low—Selection Input Voltage	Tri-State < ±20 µA		−3.3 to +5		V
Crossover High—Selection Input Voltage			−3.9 to −3.3		V
Disable Input Voltage			−5 to −3.9		V
Disable Switching Speed	50% of Input to <10% of Final V_O		980		ns
Enable Switching Speed			45		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_I = +6 V to −6 V, G = −1		40/45		ns
Output Voltage Swing		$-V_S$ + 0.10	$+V_S$ − 0.06, $-V_S$ + 0.06	$+V_S$ − 0.10	V
Short Circuit Output	Sinking and Sourcing		120		mA
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = Low		−49		dB
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			6.5	8.5	mA
Quiescent Current (Disabled)	SELECT = Low		370	500	µA
Power Supply Rejection Ratio	V_S ± 1 V	90	110		dB

[1] No sign or a plus indicates current into pin, minus indicates current out of pin.

V_S = 5 V at T_A = 25°C, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = 1, V_O = 0.2 V p-p	131	185		MHz
	G = 1, V_O = 2 V p-p	18	28		MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_O = 0.2 V p-p		12		MHz
Slew Rate	G = +1, V_O = 2 V step/G = −1, V_O = 2 V step		85/100		V/µs
Settling Time to 0.1%	G = 2, V_O = 2 V step		40		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		90		dBc
	f_C = 5 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		64		dBc
Input Voltage Noise	f = 100 kHz		4.3		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Gain Error	NTSC, G = 2, R_L = 150 Ω		0.1		%
Differential Phase Error	NTSC, G = 2, R_L = 150 Ω		0.2		Degrees
Crosstalk, Output to Output	G = 1, R_L = 100 Ω, V_{OUT} = 2 V p-p, V_S = ±5 V @ 1 MHz		−92		dB
DC PERFORMANCE					
Input Offset Voltage	SELECT = three-state or open, PNP active		200	800	µV
	SELECT = high NPN active		240	900	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2		µV/°C
Input Bias Current[1]	V_{CM} = 2.5 V, NPN active		4	6	µA
	T_{MIN} to T_{MAX}		4		µA
	V_{CM} = 2.5 V, PNP active		−8	−11	µA
	T_{MIN} to T_{MAX}		−8		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_O = 1 V to 4 V	96	105		dB
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			−0.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 2.5 V	90	105		dB
SELECT PIN					
Crossover Low, Selection Input Voltage	Three-state < ±20 µA		1.7 to 5		V
Crossover High, Selection Input Voltage			1.1 to 1.7		V
Disable Input Voltage			0 to 1.1		V
Disable Switching Speed	50% of input to <10% of final V_O		1100		ns
Enable Switching Speed			50		ns
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	V_I = −1 V to +6 V, G = −1		50/50		ns
Output Voltage Swing	R_L = 1 kΩ	$-V_S$ + 0.08	$+V_S$ − 0.04, $-V_S$ + 0.04	$+V_S$ − 0.08	V
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = low		−49		dB
Short-Circuit Current	Sinking and sourcing		105		mA
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			6	8.5	mA
Quiescent Current (Disabled)	SELECT = low		320	450	µA
Power Supply Rejection Ratio	V_S ± 1 V	90	105		dB

[1] No sign or a plus sign indicates current into the pin; a minus sign indicates current out of the pin.

V_S = 3 V at T_A = 25°C, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = 1, V_O = 0.2 V p-p	125	180		MHz
	G = 1, V_O = 2 V p-p	19	29		MHz
Bandwidth for 0.1 dB Flatness	G = 2, V_O = 0.2 V p-p		10		MHz
Slew Rate	G = +1, V_O = 2 V step/G = –1, V_O = 2 V step		73/100		V/µs
Settling Time to 0.1%	G = 2, V_O = 2 V step		48		ns
NOISE/DISTORTION PERFORMANCE					
Spurious-Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		85		dBc
	f_C = 5 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		64		dBc
Input Voltage Noise	f = 100 kHz		4.3		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Gain Error	NTSC, G = 2, R_L = 150 Ω		0.15		%
Differential Phase Error	NTSC, G = 2, R_L = 150 Ω		0.20		Degrees
Crosstalk, Output to Output	G = 1, R_L = 100 Ω, V_{OUT} = 2 V p-p, V_S = 3 V @ 1 MHz		–89		dB
DC PERFORMANCE					
Input Offset Voltage	SELECT = three-state or open, PNP active		200	800	µV
	SELECT = high NPN active		240	900	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2		µV/°C
Input Bias Current[1]	V_{CM} = 1.5 V, NPN active		4	6	µA
	T_{MIN} to T_{MAX}		4		µA
	V_{CM} = 1.5 V, PNP active		–8	–11	µA
	T_{MIN} to T_{MAX}		–8		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_O = 1 V to 2 V	90	100		dB
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		–0.2 to +3.2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	88	100		dB
SELECT PIN					
Crossover Low, Selection Input Voltage	Three-state < ±20 µA		1.7 to 3		V
Crossover High, Selection Input Voltage			1.1 to 1.7		V
Disable Input Voltage			0 to 1.1		V
Disable Switching Speed	50% of input to <10% of final V_O		1150		ns
Enable Switching Speed			50		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_I = –1 V to +4 V, G = –1		55/55		ns
Output Voltage Swing	R_L = 1 kΩ	$-V_S$ + 0.07	$+V_S$ – 0.03, $-V_S$ + 0.03	$+V_S$ – 0.07	V
Short-Circuit Current	Sinking and sourcing		72		mA
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = low		–49		dB
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			6.0	8.0	mA
Quiescent Current (Disabled)	SELECT = low		300	420	µA
Power Supply Rejection Ratio	V_S ± 1 V	88	100		dB

[1] No sign or a plus sign indicates current into the pin; a minus sign indicates current out of the pin.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$\pm V_S \pm 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8027/AD8028 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8027/AD8028. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_{S-}, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps, as discussed in the PCB Layout section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the SOIC-8 (125°C/W), SOT-23-6 (170°C/W), and MSOP-10 (130°C/W) packages on a JEDEC standard 4-layer board.

Output Short Circuit

Shorting the output to ground or drawing excessive current from the AD8027/AD8028 can likely cause catastrophic failure.

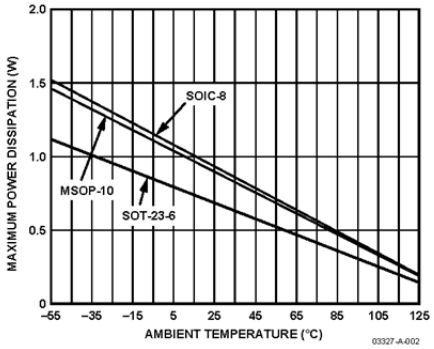


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: V_S = 5 V at T_A = 25°C, R_L = 1 kΩ, unless otherwise noted.

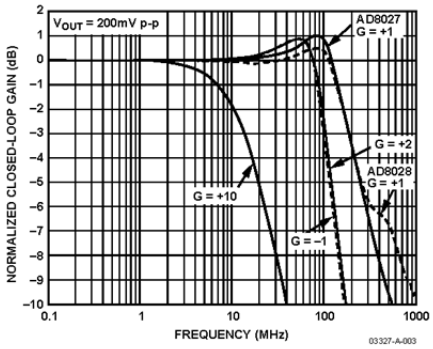


Figure 4. Small Signal Frequency Response for Various Gains

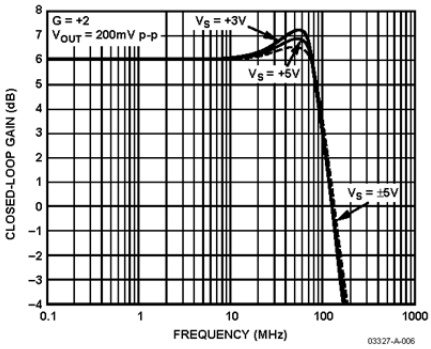


Figure 7. Small Signal Frequency Response for Various Supplies

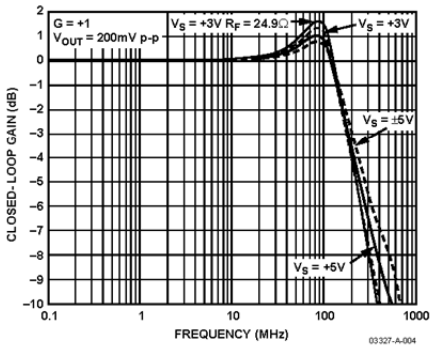


Figure 5. AD8027 Small Signal Frequency Response for Various Supplies

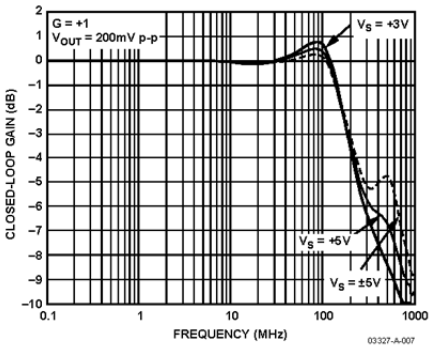


Figure 8. AD8028 Small Signal Frequency Response for Various Supplies

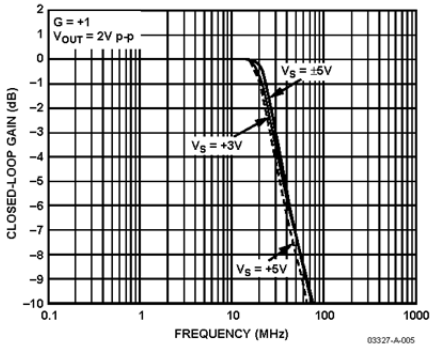


Figure 6. Large Signal Frequency Response for Various Supplies

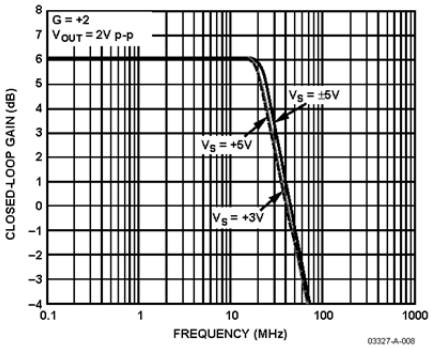


Figure 9. Large Signal Frequency Response for Various Supplies

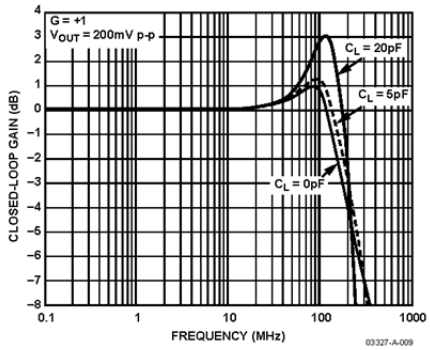


Figure 10. AD8027 Small Signal Frequency Response for Various C_{LOAD}

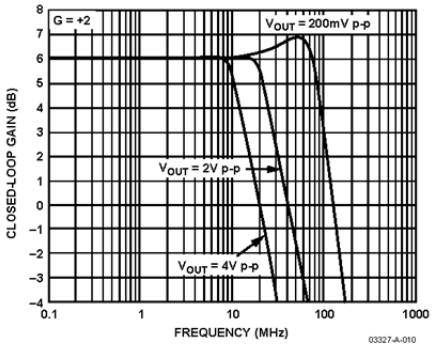


Figure 11. Frequency Response for Various Output Amplitudes

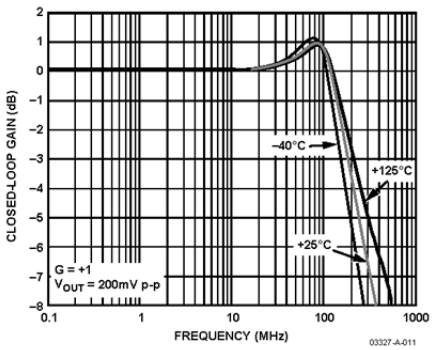


Figure 12. AD8027 Small Signal Frequency Response vs. Temperature

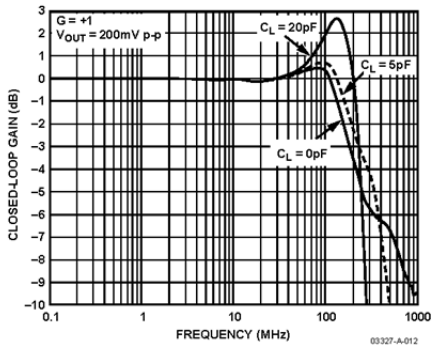


Figure 13. AD8028 Small Signal Frequency Response for Various C_{LOAD}

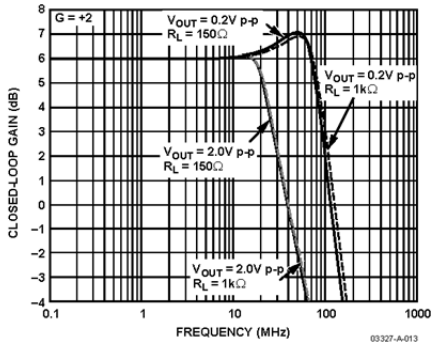


Figure 14. Small Signal Frequency Response for Various R_{LOAD} Values

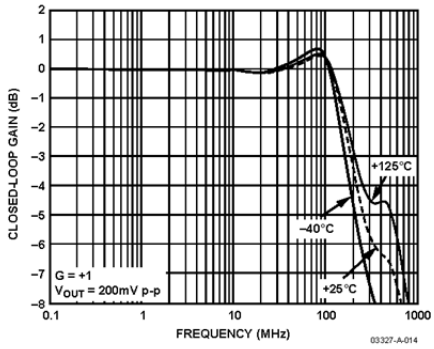


Figure 15. AD8028 Small Signal Frequency Response vs. Temperature

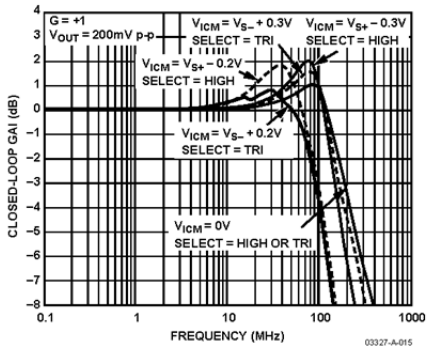


Figure 16. Small Signal Frequency Response vs. Input Common-Mode Voltages

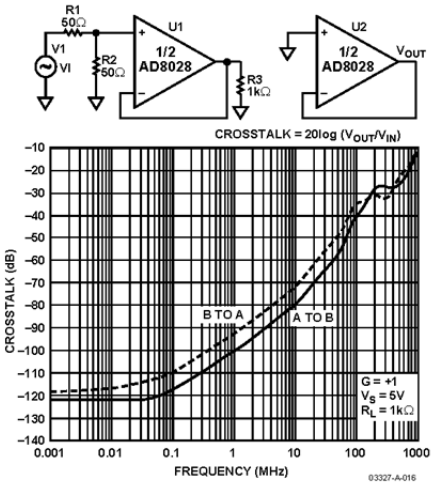


Figure 17. AD8028 Crosstalk Output to Output

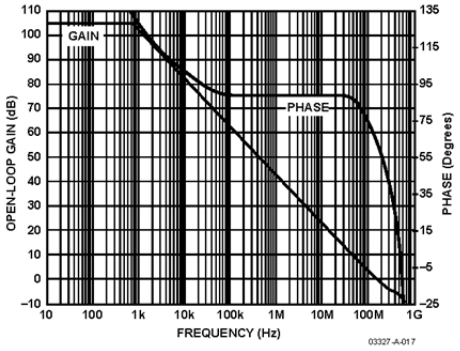


Figure 18. Open-Loop Gain and Phase vs. Frequency

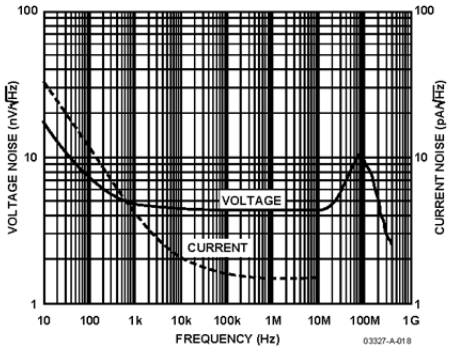


Figure 19. Voltage and Current Noise vs. Frequency

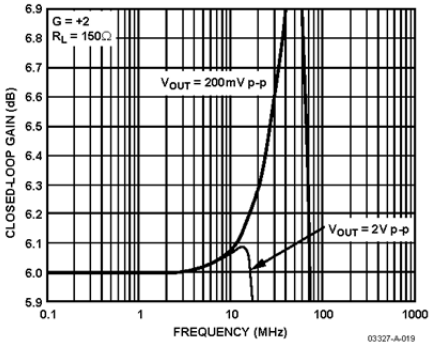


Figure 20. 0.1 dB Flatness Frequency Response

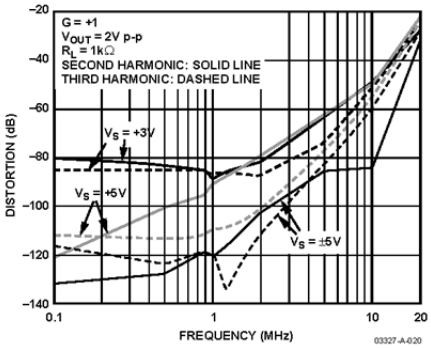


Figure 21. Harmonic Distortion vs. Frequency and Supply Voltage

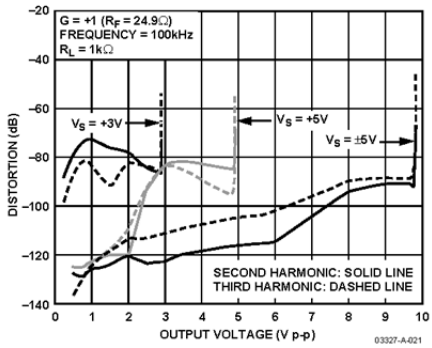


Figure 22. Harmonic Distortion vs. Output Amplitude

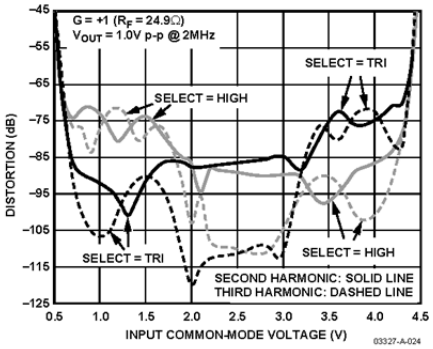


Figure 25. Harmonic Distortion vs. Input Common-Mode Voltage, V_S = 5 V

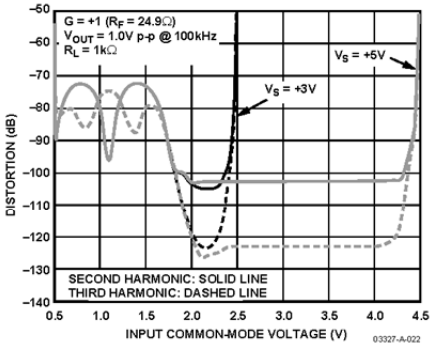


Figure 23. Harmonic Distortion vs. Input Common-Mode Voltage, SELECT = High

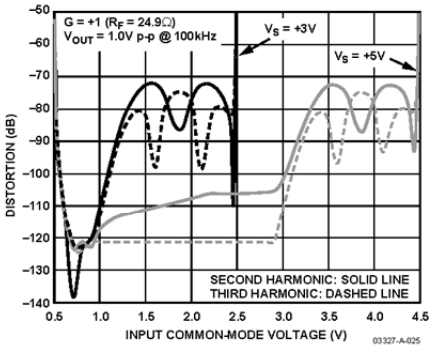


Figure 26. Harmonic Distortion vs. Input Common-Mode Voltage, SELECT = Three-State or Open

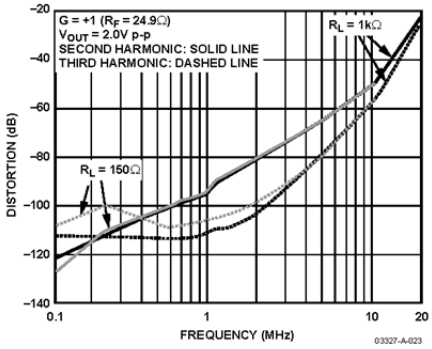


Figure 24. Harmonic Distortion vs. Frequency and Load

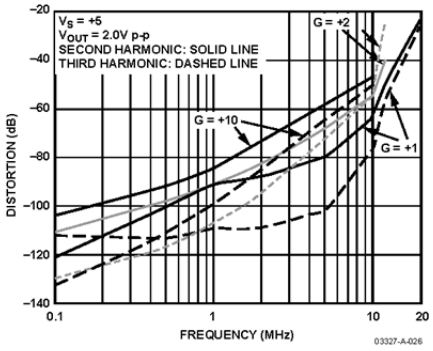


Figure 27. Harmonic Distortion vs. Frequency and Gain

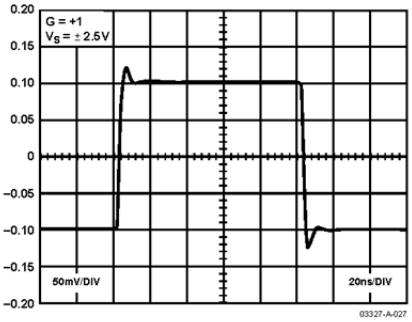


Figure 28. Small Signal Transient Response

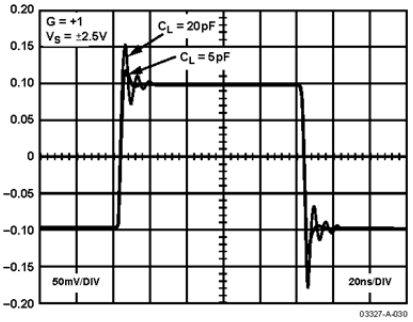


Figure 31. Small Signal Transient Response with Capacitive Load

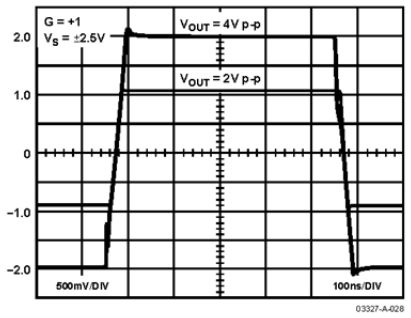


Figure 29. Large Signal Transient Response, G = +1

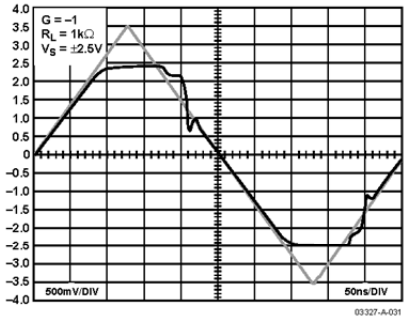


Figure 32. Output Overdrive Recovery

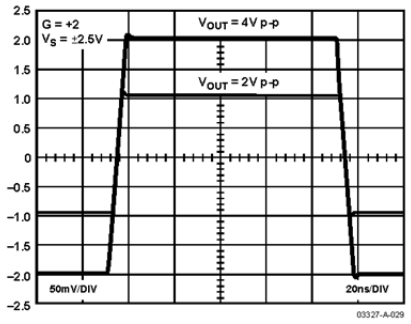


Figure 30. Large Signal Transient Response, G = +2

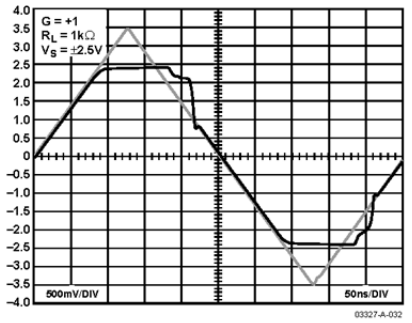


Figure 33. Input Overdrive Recovery

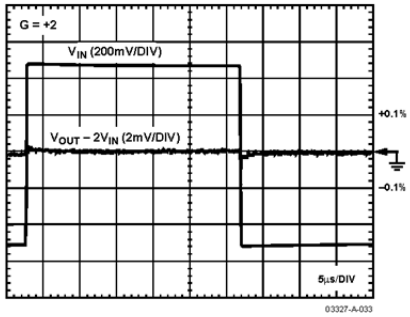


Figure 34. Long-Term Settling Time

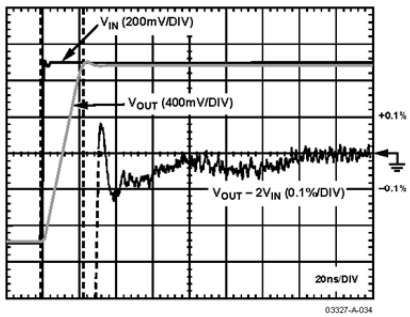


Figure 35. 0.1% Short-Term Settling Time

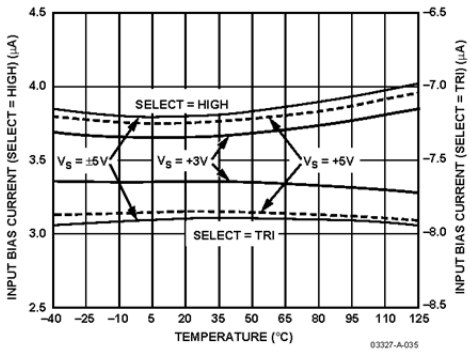


Figure 36. Input Bias Current vs. Temperature

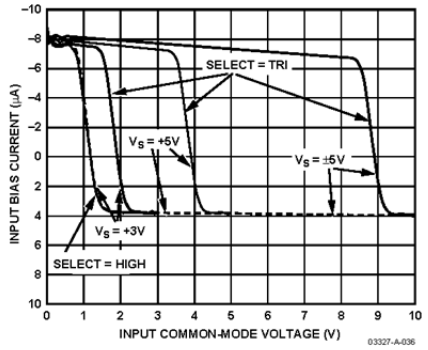


Figure 37. Input Bias Current vs. Input Common-Mode Voltage

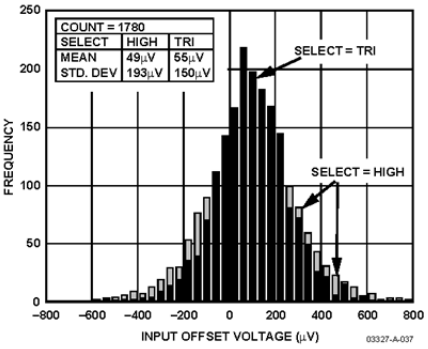


Figure 38. Input Offset Voltage Distribution

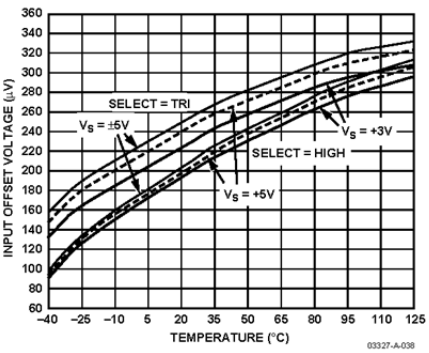


Figure 39. Input Offset Voltage vs. Temperature

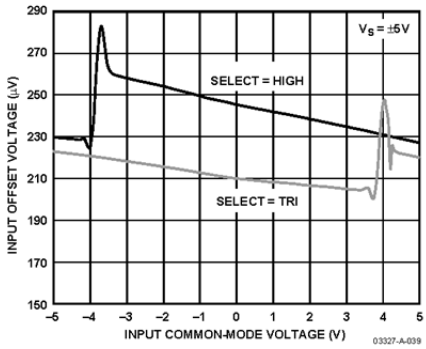


Figure 40. Input Offset Voltage vs. Input Common-Mode Voltage, V_S = ±5

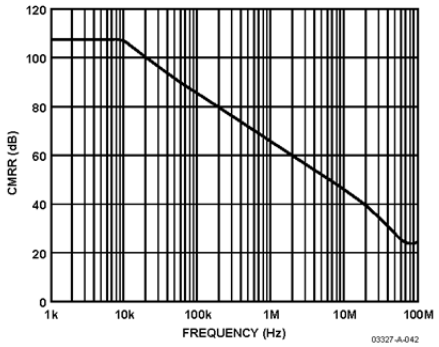


Figure 43. CMRR vs. Frequency

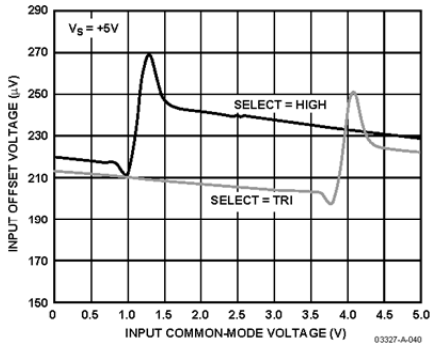


Figure 41. Input Offset Voltage vs. Input Common-Mode Voltage, V_S = 5

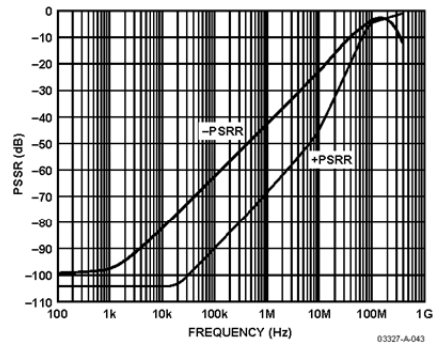


Figure 44. PSRR vs. Frequency

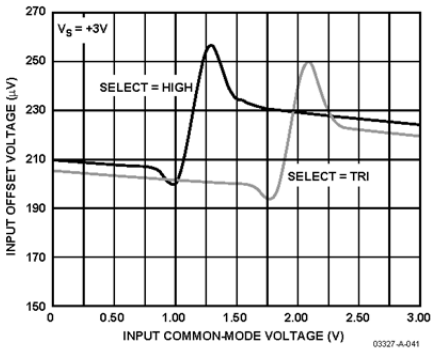


Figure 42. Input Offset Voltage vs. Input Common-Mode Voltage, V_S = 3

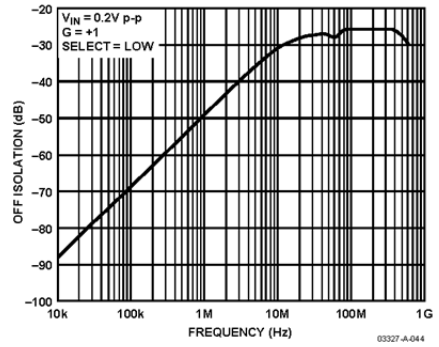


Figure 45. Off Isolation vs. Frequency

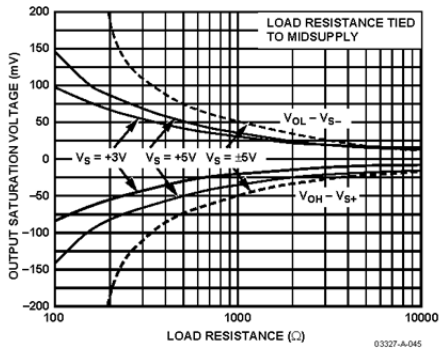


Figure 46. Output Saturation Voltage vs. Output Load

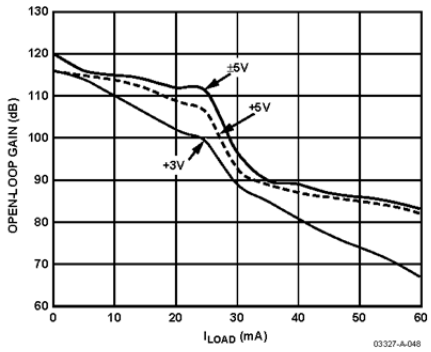


Figure 49. Open-Loop Gain vs. Load Current

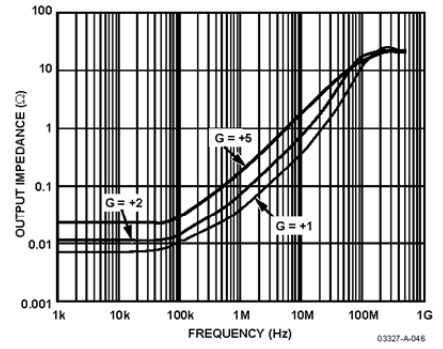


Figure 47. Output Enabled— Impedance vs. Frequency

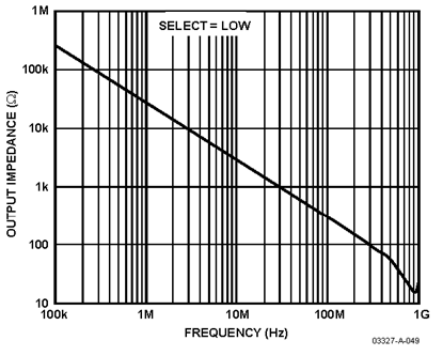


Figure 50. Output Disabled—Impedance vs. Frequency

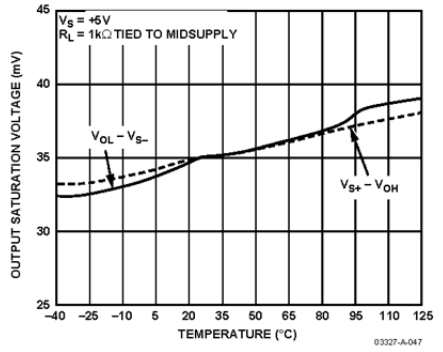


Figure 48. Output Saturation Voltage vs. Temperature

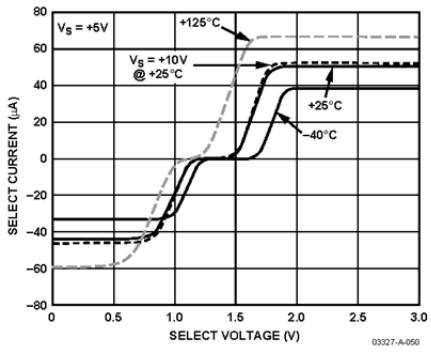


Figure 51. SELECT Pin Current vs. SELECT Pin Voltage and Temperature

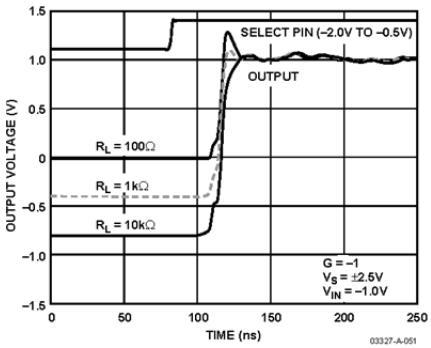


Figure 52. Enable Turn-On Timing

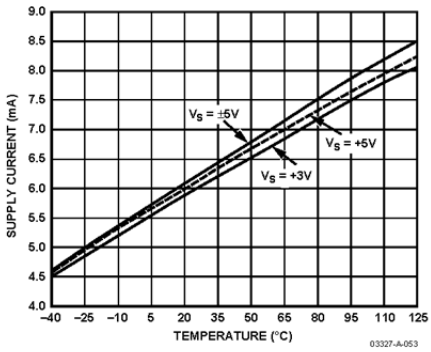


Figure 54. Quiescent Supply Current vs. Supply Voltage and Temperature

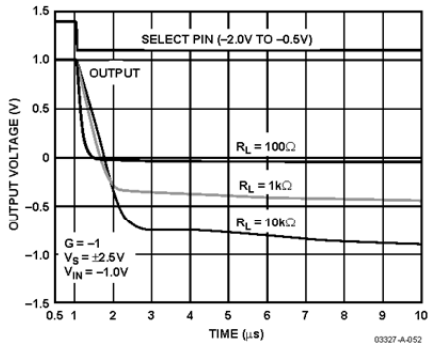


Figure 53. Disable Turn-Off Timing

THEORY OF OPERATION

The AD8027/AD8028 are rail-to-rail input/output amplifiers designed in the Analog Devices XFCB process. The XFCB process enables the AD8027/AD8028 to run on 2.7 V to 12 V supplies with 190 MHz of bandwidth and over 100 V/µs of slew rate. The AD8027/AD8028 have 4.3 nV/√Hz of wideband noise with 17 nV/√Hz noise at 10 Hz. This noise performance, with an offset and drift performance of less than 900 µV maximum and 1.5 µV/°C typical, respectively, makes the AD8027/AD8028 ideal for high speed, precision applications. Additionally, the input stage operates 200 mV beyond the supply rails and shows no phase reversal. The amplifiers feature overvoltage protection on the input stage. Once the inputs exceed the supply rails by 0.7 V, ESD protection diodes are turned on, drawing excessive current through the differential input pins. A series input resistor should be included to limit the input current to less than 10 mA.

INPUT STAGE

The rail-to-rail input performance is achieved by operating complementary input pairs. Which pair is on is determined by the common-mode level of the differential input signal. As shown in Figure 55, a tail current (I_{TAIL}) is generated that sources the PNP differential input structure consisting of Q1 and Q2. A reference voltage is generated internally that is connected to the base of Q5. This voltage is continually compared against the common-mode input voltage. When the common-mode level exceeds the internal reference voltage, Q5 diverts the tail current (I_{TAIL}) from the PNP input pair to a current mirror that sources the NPN input pair consisting of Q3 and Q4.

The NPN input pair can now operate at 200 mV above the positive rail. Both input pairs are protected from differential input signals above 1.4 V by four diodes across the input (see Figure 55). In the event of differential input signals that exceed 1.4 V, the diodes conduct and excessive current flows through them. A series input resistor should be included to limit the input current to 10 mA.

CROSSOVER SELECTION

The AD8027/AD8028 have a feature called crossover selection, which allows the user to choose the crossover point between the PNP/NPN differential pairs. Although the crossover region is small, operating in this region should be avoided, because it can introduce offset and distortion to the output signal. To help avoid operating in the crossover region, the AD8027/AD8028 allow the user to select from two preset crossover locations (voltage levels) using the SELECT pin. As shown in Figure 55, the crossover region is about 200 mV and is defined by the voltage level at the base of Q5. Internally, two separate voltage sources are created approximately 1.2 V from either rail. One or the other is connected to Q5, based on the voltage applied to the SELECT pin. This allows either dominant PNP pair operation, when the SELECT pin is left open, or dominant NPN pair operation, when the SELECT pin is pulled high.

The SELECT pin also provides the traditional power-down function when it is pulled low. This allows the designer to achieve the best precision and ac performance for high-side and low-side signal applications. See Figure 50 through Figure 53 for SELECT pin characteristics.

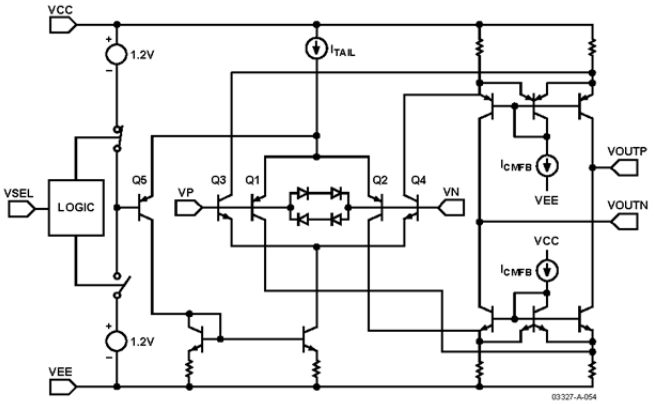


Figure 55. Simplified Input Stage

In the event that the crossover region cannot be avoided, specific attention has been given to the input stage to ensure constant transconductance and minimal offset in all regions of operation. The regions are PNP input pair running, NPN input pair running, and both running at the same time (in the 200 mV crossover region). Maintaining constant transconductance in all regions ensures the best wideband distortion performance when going between these regions. With this technique, the AD8027/AD8028 can achieve greater than 80 dB SFDR for a 2 V p-p, 1 MHz, and G = 1 signal on ±1.5 V supplies. Another requirement needed to achieve this level of distortion is that the offset of each pair must be laser trimmed to achieve greater than 80 dB SFDR, even for low frequency signals.

OUTPUT STAGE

The AD8027/AD8028 use a common-emitter output structure to achieve rail-to-rail output capability. The output stage is designed to drive 50 mA of linear output current, 40 mA within 200 mV of the rail, and 2.5 mA within 35 mV of the rail. Loading of the output stage, including any possible feedback network, lowers the open-loop gain of the amplifier. Refer to Figure 49 for the loading behavior. Capacitive load can degrade the phase margin of the amplifier. The AD8027/AD8028 can drive up to 20 pF, G = 1, as shown in Figure 10. A small (25 Ω to 50 Ω) series resistor, R_{SNUB}, should be included, if the capacitive load is to exceed 20 pF for a gain of 1. Increasing the closed-loop gain increases the amount of capacitive load that can be driven before a series resistor needs to be included.

DC ERRORS

The AD8027/AD8028 use two complementary input stages to achieve rail-to-rail input performance, as mentioned in the Input Stage section. To use the dc performance over the entire common-mode range, the input bias current and input offset voltage of each pair must be considered.

Referring to Figure 56, the output offset voltage of each pair is calculated by

$$V_{OS,PNP,OUT} = V_{OS,PNP}\left(\frac{R_G + R_F}{R_G}\right),$$

$$V_{OS,NPN,OUT} = V_{OS,NPN}\left(\frac{R_G + R_F}{R_G}\right)$$

where the difference of the two is the discontinuity experienced when going through the crossover region.

The size of the discontinuity is defined as

$$V_{DIS} = \left(V_{OS,\,PNP} - V_{OS,\,NPN}\right) \times \left(\frac{R_G + R_F}{R_G}\right)$$

Using the crossover select feature of the AD8027/AD8028 helps to avoid this region. In the event that the region cannot be avoided, the quantity ($V_{OS,\,PNP} - V_{OS,\,NPN}$) is trimmed to minimize this effect.

Because the input pairs are complementary, the input bias current reverses polarity when going through the crossover region shown in Figure 37. The offset between pairs is described by

$$V_{OS,PNP} - V_{OS,NPN} = \left(I_{B,PNP} - I_{B,NPN}\right) \times \left[R_S\left(\frac{R_G + R_F}{R_G}\right) - R_F\right]$$

$I_{B,\,PNP}$ is the input bias current of either input when the PNP input pair is active, and $I_{B,\,NPN}$ is the input bias current of either input pair when the NPN pair is active. If R_S is sized so that when multiplied by the gain factor it equals R_F, this effect is eliminated. It is strongly recommended to balance the impedances in this manner when traveling through the crossover region to minimize the dc error and distortion. As an example, assuming that the PNP input pair has an input bias current of 6 μA and the NPN input pair has an input bias current of −2 μA, a 200 μV shift in offset occurs when traveling through the crossover region with R_F equal to 0 Ω and R_S equal to 25 Ω.

In addition to the input bias current shift between pairs, each input pair has an input bias current offset that contributes to the total offset in the following manner:

$$\Delta V_{OS} = I_{B+} R_S\left(\frac{R_G + R_F}{R_G}\right) - I_{B-} R_F$$

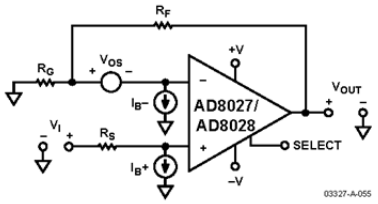


Figure 56. Op Amp DC Error Sources

WIDEBAND OPERATION

Voltage feedback amplifiers can use a wide range of resistor values to set their gain. Proper design of the application's feedback network requires consideration of the following issues:

- Poles formed by the amplifier's input capacitances with the resistances seen at the amplifier's input terminals
- Effects of mismatched source impedances
- Resistor value impact on the application's voltage noise
- Amplifier loading effects

The AD8027/AD8028 have an input capacitance of 2 pF. This input capacitance forms a pole with the amplifier's feedback network, destabilizing the loop. For this reason, it is generally desirable to keep the source resistances below 500 Ω, unless some capacitance is included in the feedback network. Likewise, keeping the source resistances low also takes advantage of the AD8027/AD8028's low input referred voltage noise of 4.3 nV/√Hz.

With a wide bandwidth of over 190 MHz, the AD8027/AD8028 have numerous applications and configurations. The AD8027/AD8028 part shown in Figure 57 is configured as a noninverting amplifier. An easy selection table of gain, resistor values, bandwidth, slew rate, and noise performance is presented in Table 5, and the inverting configuration is shown in Figure 58.

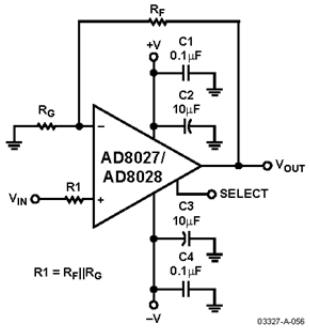


Figure 57. Wideband Noninverting Gain Configuration

Table 5. Component Values, Bandwidth, and Noise Performance (V_S = ±2.5 V)

Noise Gain (Noninverting)	R_{SOURCE} (Ω)	R_F (Ω)	R_G (Ω)	–3 dB SS BW (MHz)	Output Noise with Resistors (nV/√Hz)
1	50	0	N/A	190	4.4
2	50	499	499	95	10
10	50	499	54.9	13	45

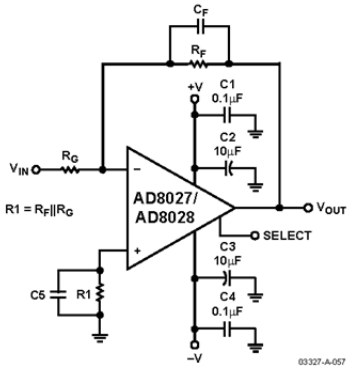


Figure 58. Wideband Inverting Gain Configuration

CIRCUIT CONSIDERATIONS

Balanced Input Impedances

Balanced input impedances can help to improve distortion performance. When the amplifier transitions from PNP pair to NPN pair operation, a change in both the magnitude and direction of the input bias current occurs. When multiplied times imbalanced input impedances, a change in offset can result. The key to minimizing this distortion is to keep the input impedances balanced on both inputs. Figure 59 shows the effect of the imbalance and degradation in distortion performance for a 50 Ω source impedance, with and without a 50 Ω balanced feedback path.

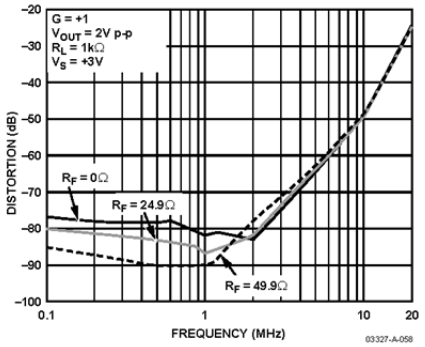


Figure 59. SFDR vs. Frequency and Various R_F

PCB Layout

As with all high speed op amps, achieving optimum performance from the AD8027/AD8028 requires careful attention to PCB layout. Particular care must be exercised to minimize lead lengths of the bypass capacitors. Excess lead inductance can influence the frequency response and even cause high frequency oscillations. The use of a multilayer board with an internal ground plane can reduce ground noise and enable a tighter layout.

To achieve the shortest possible lead length at the inverting input, the feedback resistor, R_F, should be located beneath the board and span the distance from the output, Pin 6, to the input, Pin 2. The return node of the resistor, R_G, should be situated as closely as possible to the return node of the negative supply bypass capacitor connected to Pin 4.

On multilayer boards, all layers underneath the op amp should be cleared of metal to avoid creating parasitic capacitive elements. This is especially true at the summing junction (the –input). Extra capacitance at the summing junction can cause increased peaking in the frequency response and lower phase margin.

Grounding

To minimize parasitic inductances and ground loops in high speed, densely populated boards, a ground plane layer is critical. Understanding where the current flows in a circuit is critical in the implementation of high speed circuit design. The length of the current path is directly proportional to the magnitude of the parasitic inductances and, therefore, the high frequency impedance of the path. Fast current changes in an inductive ground return can create unwanted noise and ringing.

The length of the high frequency bypass capacitor pads and traces is critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Because load currents flow from supplies as well as ground, the load should be placed at the same physical location as the bypass capacitor ground. For large values of capacitors, which are intended to be effective at lower frequencies, the current return path length is less critical.

Power-Supply Bypassing

Power-supply pins are actually inputs, and care must be taken to provide a clean, low noise, dc voltage source to these inputs. The bypass capacitors have two functions:

- Provide a low impedance path for unwanted frequencies from the supply inputs to ground, thereby reducing the effect of noise on the supply lines.
- Provide sufficient localized charge storage, for fast switching conditions and minimizing the voltage drop at the supply pins and the output of the amplifier. This is usually accomplished with larger electrolytic capacitors.

Decoupling methods are designed to minimize the bypassing impedance at all frequencies. This can be accomplished with a combination of capacitors in parallel to ground.

Good-quality ceramic chip capacitors should be used and always kept as close as possible to the amplifier package . A parallel combination of a 0.01 µF ceramic and a 10 µF electrolytic covers a wide range of rejection for unwanted noise. The 10 µF capacitor is less critical for high frequency bypassing, and, in most cases, one per supply line is sufficient.

APPLICATIONS

USING THE SELECT PIN

The AD8027/AD8028's unique SELECT pin has two functions:

- The power-down function places the AD8027/AD8028 into low power consumption mode. In power-down mode, the amplifiers draw 450 µA (typical) of supply current.
- The second function, as mentioned in the Theory of Operation section, shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail. This selectable crossover point allows the user to minimize distortion based on the input signal and environment. The default state is 1.2 V from the positive power supply, with the SELECT pin left floating or in three-state.

Table 6 lists the SELECT pin's required voltages and modes.

Table 6. SELECT Pin Mode Control

	SELECT Pin Voltage (V)		
Mode	**V_S = ±5 V**	**V_S = +5 V**	**V_S = +3 V**
Disable	−5 to −4.2	0 to 0.8	0 to 0.8
Crossover Referenced −1.2 V to Positive Supply	−4.2 to −3.3	0.8 to 1.7	0.8 to 1.7
Crossover Referenced +1.2 V to Negative Supply	−3.3 to +5	1.7 to 5.0	1.7 to 3.0

When the input stage transitions from one input differential pair to the other, there is virtually no noticeable change in the output waveform.

The disable time of the AD8027/AD8028 amplifiers is load-dependent. Typical data is presented in Table 7. See Figure 52 and Figure 53 for the actual switching measurements.

Table 7. $\overline{\text{DISABLE}}$ Switching Speeds

	Supply Voltages (R_L = 1 kΩ)		
Time	**±5 V**	**+5 V**	**+3 V**
t_{ON}	45 ns	50 ns	50 ns
t_{OFF}	980 ns	1100 ns	1150 ns

DRIVING A 16-BIT ADC

With the adjustable crossover distortion selection point and low noise, the AD8028 is an ideal amplifier for driving or buffering input signals into high resolution ADCs such as the AD7767, a 16-bit, 1 LSB INL, 1 MSPS differential ADC. Figure 60 shows the typical schematic for driving the ADC. The AD8028 driving the AD7677 offers performance close to non-rail-to-rail amplifiers and avoids the need for an additional supply other than the single 5 V supply already used by the ADC.

In this application, the SELECT pins are biased to avoid the crossover region of the AD8028 for low distortion operation.

Summary test data for the schematic shown in Figure 60 is listed in Table 8.

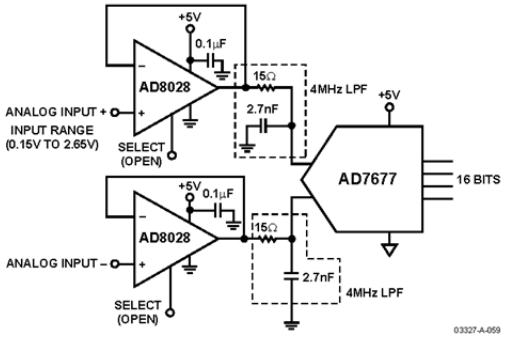


Figure 60. Unity Gain Differential Drive

Table 8. ADC Driver Performance, f_C = 100 kHz, V_{OUT} = 4.7 V p-p

Parameter	**Measurement**
Second Harmonic Distortion	−105 dB
Third Harmonic Distortion	−102 dB
THD	−102 dB
SFDR	+105 dBc

As shown in Figure 61, the AD8028 and AD7677 combination offers excellent integral nonlinearity (INL).

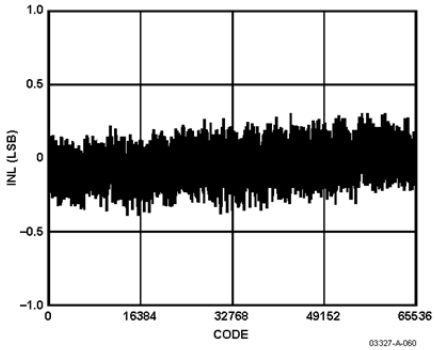


Figure 61. Integral Nonlinearity

BAND-PASS FILTER

In communication systems, active filters are used extensively in signal processing. The AD8027/AD8028 are excellent choices for active filter applications. In realizing this filter, it is important that the amplifier have a large signal bandwidth of at least 10× the center frequency, f_O. Otherwise, a phase shift can occur in the amplifier, causing instability and oscillations.

In Figure 62, the AD8027/AD8028 part is configured as a 1 MHz band-pass filter. The target specifications are f_O = 1 MHz and a −3 dB pass band of 500 kHz. To start the design, select f_O, Q, C1, and R4. Then use the following equations to calculate the remaining variables:

$$Q = \frac{f_O\ (\text{MHz})}{Band\ Pass\ (\text{MHz})}$$

$$k = 2\pi f_O C1$$

$$C2 = 0.5C1$$

$$R1 = 2/k,\ R2 = 2/(3k),\ R3 = 4/k$$

$$H = 1/3(6.5 - 1/Q)$$

$$R5 = R4/(H - 1)$$

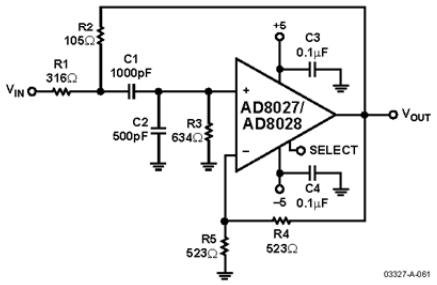


Figure 62. Band-Pass Filter Schematic

The test data shown in Figure 63 indicates that this design yields a filter response with a center frequency of f_O = 1 MHz, and a bandwidth of 450 kHz.

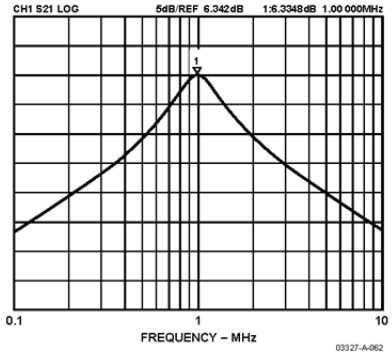
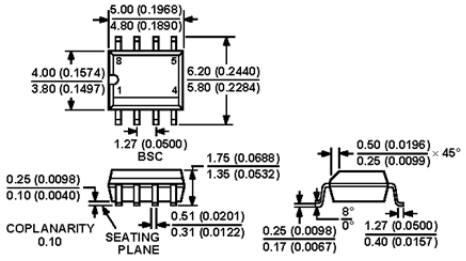


Figure 63. Band-Pass Filter Response

DESIGN TOOLS AND TECHNICAL SUPPORT

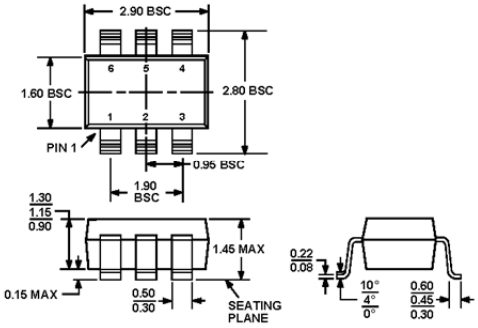
Analog Devices, Inc. (ADI) is committed to simplifying the design process by providing technical support and online design tools. ADI offers technical support via free evaluation boards, sample ICs, interactive evaluation tools, data sheets, spice models, application notes, and phone and email support available at www. analog.com.

OUTLINE DIMENSIONS



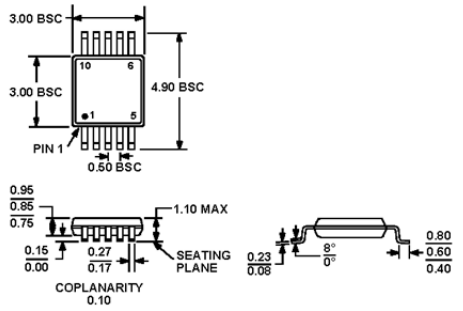
COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 64. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178AB

Figure 65. 6-Lead Small Outline Transistor Package [SOT-23]
(RT-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187BA

Figure 66. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Minimum Ordering Quantity	Temperature Range	Package Description	Package Option	Branding
AD8027AR	1	–40°C to +125°C	8-Lead SOIC	R-8	
AD8027AR-REEL	2,500	–40°C to +125°C	8-Lead SOIC	R-8	
AD8027AR-REEL7	1,000	–40°C to +125°C	8-Lead SOIC	R-8	
AD8027ARZ[1]	1	–40°C to +125°C	8-Lead SOIC	R-8	
AD8027ARZ-REEL[1]	2,500	–40°C to +125°C	8-Lead SOIC	R-8	
AD8027ARZ-REEL7[1]	1,000	–40°C to +125°C	8-Lead SOIC	R-8	
AD8027ART-R2	250	–40°C to +125°C	6-Lead SOT-23	RT-6	H4B
AD8027ART-REEL	10,000	–40°C to +125°C	6-Lead SOT-23	RT-6	H4B
AD8027ART-REEL7	3,000	–40°C to +125°C	6-Lead SOT-23	RT-6	H4B
AD8027ARTZ-R2[1]	250	–40°C to +125°C	6-Lead SOT-23	RT-6	H4B#
AD8027ARTZ-REEL[1]	10,000	–40°C to +125°C	6-Lead SOT-23	RT-6	H4B#
AD8027ARTZ-REEL7[1]	3,000	–40°C to +125°C	6-Lead SOT-23	RT-6	H4B#
AD8028AR	1	–40°C to +125°C	8-Lead SOIC	R-8	
AD8028AR-REEL	2,500	–40°C to +125°C	8-Lead SOIC	R-8	
AD8028AR-REEL7	1,000	–40°C to +125°C	8-Lead SOIC	R-8	
AD8028ARZ[1]	1	–40°C to +125°C	8-Lead SOIC	R-8	
AD8028ARZ-REEL[1]	2,500	–40°C to +125°C	8-Lead SOIC	R-8	
AD8028ARZ-REEL7[1]	1,000	–40°C to +125°C	8-Lead SOIC	R-8	
AD8028ARM	1	–40°C to +125°C	10-Lead MSOP	RM-10	H5B
AD8028ARM-REEL	3,000	–40°C to +125°C	10-Lead MSOP	RM-10	H5B
AD8028ARM-REEL7	1,000	–40°C to +125°C	10-Lead MSOP	RM-10	H5B
AD8028ARMZ[1]	1	–40°C to +125°C	10-Lead MSOP	RM-10	H5B#
AD8028ARMZ-REEL[1]	3,000	–40°C to +125°C	10-Lead MSOP	RM-10	H5B#
AD8028ARMZ-REEL7[1]	1,000	–40°C to +125°C	10-Lead MSOP	RM-10	H5B#

[1] Z = Pb-free part, # denotes lead-free, may be top or bottom marked.

LIST OF REFERENCES

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